International Conference on IC Design & Technology

Minatec Grenoble, France
June 2nd – June 4th , 2008
www.ICICDT.org

Conference Vision

Global collaboration among professionals engaged in the multi-disciplinary fields of advanced IC design, device design, design tools/technology and process technology development enables accelerated product time-to-market, particularly for high-performance products which incorporate advanced management of power, leakage, device degradation and yield.

Conference overview

ICICDT provides a forum for engineers, researchers, scientists, professors and students to explore the interactions of design and process technology on product/IC development & manufacturing. The unique workshop style of the conference and the unusual opportunity for technologists and product designers to interact enables the exchange of breakthrough ideas and creative collaboration. Two days of technical presentations and workshops will be preceded by a one-day tutorial program of value to both the expert and the beginner.

Close collaboration amongst professionals in the multi-disciplinary technical fields - design/device/process - accelerates the implementation of new designs and new technologies into manufacturing. The separation of system/IC design and manufacturing in the semiconductor industry - leading to the emergence of specialized fabless design houses, wafer foundries, design automation tool/software companies, and semiconductor processing tool suppliers - creates a need for collaboration among individuals with technical skills across these multiple fields. Further, advanced IC technology can no longer offer the same level of control as earlier over many parameters that have a direct adverse impact on circuit behavior. New IC designs also push the limit of technology, and in some cases, require specific fine-tuning of certain process modules in manufacturing.

Thus the communities of design and technology are increasingly intertwined. The issues which require close interaction and collaboration for trade-off and optimization across the design/device/process fields are addressed in this conference. Hence, this conference is organized in a session format with 82 invited and contributed talks, to provide opportunities for a direct interaction among the attendees and presenters, to participate in discussions across multiple disciplines of design/device/process issues during the two days of 14 plenary & workshop sessions. Each session is organized with short oral presentations followed by a one-hour workshop to facilitate interactive discussion of questions & answers. In addition, on the first day, eight in-depth tutorial courses have been organized.

Who Should Attend?

This conference is intended for IC design, circuit, device, process, integration, and reliability engineers and managers working to accelerate the product time-to-market through the implementation of new designs and new technologies into manufacturing, including the design and development of advanced devices and materials, and IC and device reliability.

Conference Venue

The venue for the 2008 Conference is Minatec at Grenoble, France.

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June 2 – 4, Minatec, Grenoble, France ; http://www.ICICDT.org

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- Samukawa Seiji, Tohoku University, Japan
- Scarpa Andrea, NXP Semiconductors, The Netherlands
- Shuto Susumu, Toshiba, Japan
- Stinson Jason, Intel, USA
- Sumita Masaya, Panasonic-Matsushita Electric Industrial Co.LTD, Japan
- Takayanagi Toshinari, P. A. Semi, USA
- Van den Bosch Geert, IMEC, Belgium
- Yeap Geoffrey, Qualcomm, USA
- Young Chadwin, Sematech, USA
- Zhang Ming, Intel, USA

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ICICDT Tutorials

Tutorial Chair: Ali Keshavarzi, Intel, USA

June 2, 2008

Tutorial A	*Future Technologies and Devices*
8:30 a.m	**Registration**
9:00 a.m	**CMOS Device Scaling for 45nm Node and Beyond** Tahir Ghani, Intel Corporation, USA
10:30 a.m	**Coffee Break**
10:45 a.m	**Low-Voltage Scaling Limitations of Nano-Scale CMOS LSIs** Kiyoo Itoh, Hitachi, Japan
12:15 p.m	**Lunch**
2:00 p.m	**Spintronics – is it the electronics of the future?** Stu Wolf, The University of Virginia, USA
3:30 p.m	**Coffee Break**
3:45 p.m	**Towards Bottom-up Nanoelectronics?** Jean-Philippe Bourgoin, CEA-LEM, France
5:15 p.m	**Adjourn**

CMOS Device Scaling for 45nm Node and Beyond

In this tutorial I will describe the barriers to scaling conventional transistors and follow this discussion by presenting various innovations which circumvent these barriers. I will discuss how innovations such as uniaxially-strained silicon and "HiK+Metal Gate" technologies have enabled dramatic performance enhancement for the recent CMOS nodes and describe specific challenges which had to be overcome to expedite their implementation into mainstream CMOS manufacturing. I will also discuss the role of increasing power density, device variability and transistor parasitcs in limiting future CMOS transistor scaling and show how innovations such as Muti-Gate structure and high mobility alternative channel materials have the potential to successfully address upcoming scaling challenges in a power-limited era.

Tahir Ghani is an Intel Fellow and Director of Transistor Technology and Integration at Intel Corporation. Since joining Intel in 1994, he has led the teams responsible for developing some of the most significant changes in semiconductor industry and implementing them into mainstream CMOS manufacturing. Tahir co-led the team responsible for developing industry-first HiK Metal Gate CMOS technology for Intel's 45nm technology node. He also led the team responsible for developing industry-first strained Silicon CMOS technology for Intel's 90nm technology node. He is currently leading transistor technology development for 22nm CMOS logic node. Tahir received his PhD in Electrical Engineering from Stanford University. He has received Intel's highest technical award (Intel Achievement Award) twice for his work on transistor development.

Low-Voltage Scaling Limitations of Nano-Scale CMOS LSIs

In this tutorial, low-voltage scaling limitations of nano-scale CMOS LSIs are described, focusing on specific circuit blocks such as logic gates, SRAM cells, and DRAM sense amplifiers.

First, a new evaluation methodology of the minimum V_{DD} (V_{min}) of LSIs, based on tolerable speed variations, is proposed and the low-voltage limitations of each block are then compared by using the methodology. It turns out that V_{min} strongly depends on the ever-larger V_T variation and rapidly increases with device scaling. In addition, the 6-T SRAM cell gives the low-voltage limitation of LSIs with the highest V_{min}. Second, possible solutions to drastically reduce V_{min} are presented and evaluated. They are repair techniques, new MOSFETs (e.g., metal-gate bulk and metal-gate FD-SOI), and low-V_T dynamic circuits. It is also shown that the V_{min} of the twin-DRAM cell combined with the full-V_{DD} sensing gives the lowest V_{min}, implying that it will attract more attention for low-voltage low-cost LSIs. After that, future prospects are given.

Kiyoo Itoh is currently a Hitachi Fellow. He was a Visiting MacKay Lecturer at U.C. Berkeley in 1994, a Visiting Professor at the University of Waterloo in 1995, and a Consulting Professor at Stanford University in 2000-2001. He was a Member of the IEEE Fellow Committee from1999 to 2002, and an elected AdCom Member of IEEE Solid-State Circuits Society from 2001 to 2003. He is a Distinguished Lecturer of the IEEE Solid-state Circuits Society. Since 1972 he has led low-power/low-voltage RAM circuits at Hitachi Ltd: He was the lead designer of the first prototype for eight generations of Hitachi DRAMs ranging from 4 Kbits to 64 Mbits. In the course of the developments he invented in 1974 the concept of folded data-line (i.e., bit-line) arrangement, which uses a pair of balanced data lines to eliminate various noise components, and presented the

architecture for a 64-Kbit DRAM at the 1980 ISSCC. Since that time, this architecture has been adopted for nearly all DRAM chips since produced. He went on to develop high-density DRAM devices, and low-power/low-voltage DRAM circuits and array architectures. They are triple-well substrate, advanced three-dimensional capacitors, pipe-lined DRAMs, on-chip substrate-bias generators, half-VDD sensing, on-chip voltage-down converters enabling the aging (burn-in) stress test, PMOS word driver, the so-called CMOS direct sensing, multi-divided data-lines, transposed data-lines, low-voltage charge pump, and stress-voltage tolerated I/O circuits. Many of them have been de-facto standards. In addition, as early as 1988, as a pioneer, he initiated circuit inventions and developments to reduce subthreshold current of MOSFETs even for the active mode, which is highlighted today in low-voltage CMOS LSI designs. Typical examples of the reduction circuits are multi-threshold (VT) CMOS logic, various gate-source (self and offset) back-biasing schemes, multi-divided power line schemes, and power switches that we take for granted today. His current interest is in adaptive circuits to cope with variability in the nano-scale LSI era. He holds over 430 patents in Japan and US. He authored four books and three book chapters on memory designs, and contributed over 130 technical papers and presentations, many of them invited, in IEEE journals and conference proceedings. Dr. Itoh has won many honors. They include the IEEE Paul Rappaport Award in 1984, the Best Paper Award of ESSCIRC90, the 1993 IEEE Solid-State Circuits Award, and the 2006 IEEE Jun-ichi Nishizawa Medal. He is an IEEE Fellow. In Japan, his awards include the National Medal of Honor with Purple Ribbon from the Japanese Emperor in 2000.

Spintronics – is it the electronics of the future?

In this tutorial I will cover the basic concepts of spin dependent transport including Giant Magneto-Resistance (GMR) and Spin Dependent Tunneling (SDT). I will describe the development of the first Magnetic Random Access memory Chip by Motorola/Freescale. I will describe the limitations of this technology and then describe the discovery and state of the art of Spin Torque Transfer Switching that offers a potential solution to the problem of scaling MRAM to the 45nm and 32nm lithographic nodes. Finally I will discuss the application of spintronics to logic devices including description of various concepts for spin transistors, spin wave devices and spin exchange switches which have the potential for very low power dissipation and high speed.

Stu Wolf is currently the Director of the University of Virginia Institute for Nanoscale and Quantum Scientific and Technological Advanced Research (nanoSTAR) and also serves as a professor in the Materials Science and Engineering Department as well as the Physics Department. Stu Wolf was previously a Program Manager at DARPA and a Senior Scientist at the Naval Research Laboratory. At DARPA he conceived and initiated several projects on functional materials that pushed the frontiers of materials science for electronics and he both started the Spintronics program (and invented the word "spintronics") to develop Magnetic Random Access Memory (MRAM). At the University of Virginia he is continuing to push the frontiers in spintronics and quantum information science. His group will be utilizing the spin degree of freedom in novel heterostructures using spin torque to manipulate the magnetism in nanomagnetic structures. He also will be developing a new spintronic logic based on controlling the exchange in magnetic quantum dots. He has an AB from Columbia College (64) and an MS (66) and PhD (69) from Rutgers University. He was a Research Associate at Case Western Reserve University (70-73) and a Visiting Scholar at UCLA (81-82). He is a Fellow of the APS (84), and was a Divisional Councilor for the Condensed Matter Division (90-91) and for the Forum on Industrial and Applied Physics. He has authored or co-authored two books over 300 articles and has edited numerous conference proceedings.

Towards Bottom-up Nanoelectronics?

In this tutorial, I will first discuss the framework of the nanoelectronics evolution that call for introduction of both evolutionary and disrupting technologies. I will consider in particular the attempts made to develop bottom-up electronics within that framework. I will then present the key objects (nanotubes, nanowires, molecules, quantum dots, bio-objects) and concepts (self and directed assembly) of the bottom-up nanofabrication approaches. Examples of devices, functions and circuits realized using such objects and concepts will then be presented and discussed. Finally, I will outline the main roadblocks towards large scale application of bottom-up concepts.

Bio **Jean-Philippe Bourgoin** …

Tutorial B *Future Circuits and Design Challenges*

8:30 a.m	**Registration**
9:00 a.m	**CMOS Proximity Communications for 3D System Integration** Tadahiro Kuroda, Keio University,

	Japan
10:30 a.m	**Coffee Break**
10:45 a.m	**Assessment of New Process Technologies at the System Level** Phillip Christie, NXP Semiconductors, Belgium
12:15 p.m	**Lunch**
2:00 p.m	**Read-out and Sense Circuit for Bio Chips and Label-less DNA Detection** Daniela De Venuto, Politecnico Di Bari, Italy
3:30 p.m	**Coffee Break**
3:45 p.m	**Technology Impacts on Future Memory Circuits** Dinesh Somasekhar or Ali Keshavarzi, Intel Corporation, USA
5:15 p.m	**Adjourn**

CMOS Proximity Communications for 3D System Integration

Scaling of CMOS integrated circuits is becoming difficult due to increase in power dissipation and device variations. Two future directions in IC technology are in prospect; “More Moore” by the conventional device scaling and “More than Moore” by System-in-Package (SiP). This lecture will present some of the recent research achievements on 3D system integration by SiP. Especially focus will be placed on CMOS proximity inter-chip communications. Capacitive and inductive coupling I/Os are emerging non-contact parallel links for chips that are stacked in a package. They are implemented by digital circuits in a standard CMOS. No new wafer process or mechanical process is required, and hence inexpensive. Since there is no pad exposed for contact, ESD protection structure can be removed. Chips under difference supply voltages can be directly connected, because they provide with an AC-coupling interface. In the lecture, fundamental differences between the inductive coupling and the capacitive coupling will be discussed. Advantages of the inductive coupling over Through-Silicon-Vias and micro-bumps will then be referred to. Circuit techniques to raise aggregated data rate to 1Tb/s, perform burst data transmission at 11Gb/s/channel, lower energy dissipation to 0.1pJ/b, and extend communication ranges over 1mm will be presented. Lastly, future challenges and opportunities such as a 3D scaling scenario will be described.

Tadahiro Kuroda received the Ph.D. degree in EE from the University of Tokyo. From 1982 to 2000 he was with Toshiba Corporation, where he designed CMOS/BiCMOS/ECL SRAMs, ASICs, ASSPs. From 1988 to 1990, he was a Visiting Scholar with the University of California, Berkeley, where he conducted research in the field of VLSI CAD. He invented a Variable Threshold-voltage CMOS technology and a Variable Supply-voltage scheme in 1996. In 2000, he moved to the Keio University, and he has been a professor since 2002. He is a Visiting MacKay Professor at the University of California, Berkeley. His research interests include low-power, high-speed CMOS design for wireless and wireline communications, human computer interactions, and ubiquitous electronics. He has published more than 200 technical publications including 50 invited papers and 18 books/chapters, and filed more than 100 patents. He served as a conference/TPC chair/member of IEEE conferences such as Symp. on VLSI Circuits, CICC, A-SSCC, DAC, ASP-DAC, ICCAD, ISLPED. He is an IEEE Fellow, an elected AdCom member for the IEEE Solid-State Circuits Society and an IEEE SSCS Distinguished Lecturer.

Assessment of New Process Technologies at the System Level

As ever more complex System-on-Chip designs are attempted and devices display increasingly non-ideal behavior, the sequence of “abstraction walls” separating design from technology must continually be reinforced. This has resulted in such complex design flows that it has become impractical to perform meaningful experiments at the interface between design and technology. In this tutorial, we present several options for simplified design flows, specifically targeted for rapid system-level technology evaluation. The tutorial will begin with a review of traditional metrics for device technology evaluation (intrinsic gate delay, ring oscillator performance) and an assessment of their strengths and weaknesses. Next, an open-source MATLAB-based toolbox called PSYCHIC (Parametric SYstem-level CHaracterization of Integrated Circuits) for rapid system level technology pathfinding will be introduced. The toolbox is designed on the assumption that it is impossible to create a single, stand-alone program to suit all technology assessments needs. Instead, the approach is to create a set of basic modelling functions (timing, routing, power analysis) and for the user of the toolbox to write their own scripts within the Matlab programming environment. Finally, a more sophisticated flow based on rapid standard cell library generation/characterization software will be discussed and examples from assessment exercises at the 32nm node on large IP blocks will be presented.

Phillip Christie received his Ph.D. in molecular electronics from the University of Durham, UK, in 1985. After a post-doctoral appointment, he joined

the faculty of the Electrical and Computer Engineering Department at the University of Delaware in 1986, where he developed a research group focussed on design, modelling and metrology of electronic and optical interconnect-limited computer systems. Following a sabbatical years at the University of Southampton in 1997 and Philips Research in 2000, he accepted a position at Philips Research in Leuven, Belgium in 2002, which became NXP Semiconductors in 2006 with the spin-off of Philip's semiconductor division. He currently holds the position of senior principal scientist in the process technology sector, with responsibilities for ultra-low power CMOS development, design-technology integration, and strategic planning.

Read-out and Sense Circuit for Bio Chips and Label-less DNA Detection

Continuing technological improvements are opening new areas of application in micro- and nano-electronics and photonics. Micro- and nano-sensor systems include on the same die or in the same packaging also the post-processing electronics for a wide range of applications. Many systems are accommodated in remote or noisy locations, e.g. industrial process control, automotive systems, space aircrafts, as well as in biomedical, particle physics and electrochemical systems. The environmental conditions may be very harsh reducing the overall lifetime due to fast ageing, thus determining the performance degradation. Post-processing may also degrade the performance of the sensor system.

Although significant advances have been reported over the last two decades, many problems are still unsolved. Modeling, design procedures and fabrication techniques are open for research, while industrial interest is aiming to satisfying technological, costing and manufacturing requirements. The aim of the tutorial is to provide examples of applications in the area of sensors and sensor interfaces on the base of experience done in the field of high energy physics measurements, domestic power measurements, biomedical applications.

Daniela De Venuto graduated in Electronic Engineering at the Politecnico di Bari, Italy, in 1989 where she received the PhD degree in 1992. In 1993 Dr. De Venuto took a post-doctoral position at the Politecnico di Bari and since 1993 she is member of (National Institute of Nuclear Physics) INFN working on silicon drift detector design (DSI Project) and in design and test of radiation hardened analogue front-ends for pixel-detector (ALICE project) developing part of research activity at CERN, Geneva, Switzerland. She became assistant professor in 1994 at the University of Lecce, Italy and then in Bari in 1999. In 2000 Dr. De Venuto was on sabbatical leave working at the Laboratoire d'Electronique Generale of the Ecole Fédéral de Lausanne (EPFL), Switzerland. During this stay she worked in the area of Hall sensor interface design in FD SOI technology. Since 2002 she is Visiting Scholar at the University of Washington, Seattle (USA) and Visiting Professor at the Lancaster University (UK). Since 2003 she is Associate Professor at the Politecnico di Bari teaching courses in Analog Electronics and Design of Integrated Circuits and System. Prof. De Venuto is co-author of more than 100 papers on major international Journals and conference Proceedings and of a patent on fully digital technique to test Sigma-Delta ADC in collaboration with the Politecnico di Torino. Her research interests include the design and test of analogue ICs, design for testability for analogue and mixed-signal circuits as well as characterisation of sensors.

Technology Impacts on Future Memory Circuits

Technology scaling has enabled high performance ICs that require large on-die caches with the trend pointing to even larger cache sizes to meet server-class workloads. Furthermore, Multi-core systems have exacerbated the problem of providing adequate memory bandwidth to the cores. As silicon technology continues to scale, the possibility of fabricating dense memories operating at low supply voltages with minimal process cost impact is of great interest. Meanwhile the increased parameter variations are posing great challenges in today's SRAM cache memory design limiting its operation at low supply voltage. This tutorial explores the impacts and interactions of technology with memory circuits.

Ali Keshavarzi is a senior research scientist at Intel Corporation's Circuit Research Laboratories (CRL) at Portland, Oregon. He is currently working on circuits and systems with various nanotechnology devices including high mobility materials such as Carbon Nanotubes. Ali is also interested in emerging dense memory circuits and technologies. Ali has also worked and is interested in research and development in the area of low-power/high-performance circuit techniques and transistor device structures for future generations of microprocessors. Ali received his Ph.D. degree in electrical engineering from Purdue University, West Lafayette, Indiana. He has published more than 45 papers and has more than 35 issued patents and more than 15 pending patents. Ali has received the best paper award at 1997 IEEE International Test Conference at Washington, D.C. on testing solutions of intrinsically leaky integrated circuits. Ali is a member of the ISLPED (International Symposium on Low Power Electronics and

Design) technical program committee. Ali has been leading the technology and circuits technical committee of ISLPED and is the chair of the technical program committee of ISLPED for 2007. Ali is an adjunct faculty at Purdue University and also teaches at Portland State University. He has co-advised Ph.D. students at Purdue University, University of Washington, University of Arizona and University of Waterloo.

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Keynotes

A Futur View of SoC in the Post 45nm era

Dr Uming Ko, TI Senior Fellow, USA

Abstract

While the semiconductor industry has delivered tremendous advancements over the years, the 45nm process node era is still in its infancy with only <20% of the market actually utilizing this process node by 2010. There are still many, many more benefits to be realized from 45nm technology. Over the last two decades of semiconductor process technology advancements, the electronics industry has enjoyed continuous improvements in performance, reduction in power and reduction in die size. And, these trends are expected to continue into the future as the industry moves into 45nm and beyond.

Dr. Uming Ko, Senior Fellow and Director of Wireless Chip Technology Center from Texas Instrument's will talk about the future trends expected in the post 45nm era of process technology, continued improvements in performance, power and size. He will also assess the characteristics of different end products such as wireless handsets, advanced imaging and surveillance and medical electronics, to determine which semiconductor products and markets might be good candidates for driving advanced process nodes. Advanced process nodes beyond 45nm will continue to deliver the types of advancements we've experienced historically; however going forward there is an increasing need to assess which products make sense for advanced nodes regardless of what is technically feasible. Dr. Ko will evaluate SoC trends going forward and will discuss the broader, market-based considerations for technology decisions in the post 45nm era.

Synergy between design and process: a key factor in the evolving microelectronic landscape.

Michel Brillouët, CEA-LETI Deputy Manager, France

Abstract

In scaling down the dimensions of the transistors in integrated circuits, major issues need to be solved. As we approach the resolution limit of the lithographic tool, extensive modifications of the patterns need to be performed on the mask in order to match the expected features on the circuit. More and more trade-offs need to be addressed in designing complex circuits like power consumption, variability, error rate, etc.: a better interplay between the technology constraints and the design complexity has to be developed. Moving to non conventional CMOS (e.g. FinFET) induces specific issues to be dealt with through the design style. On the far end of this spectrum emerging research devices and architectures, as they are called in the ITRS roadmap, may need 'out-of-the box' thinking in the way complex systems and applications will be integrated.

Besides the pure scaling for performance enhancement one observe a diversification of the devices and functions to be integrated in a circuit or in a package: this major trend called 'More-than-Moore' calls also for new design methods.

Finally the microelectronics industry itself experiences a major restructuring, especially with the emergence of the foundry model. How the technical and economical factors could interact in the future will be discussed in the later part of the presentation.

Biography

Michel Brillouët joined CEA-LETI in 1999 where he managed a R&D division on silicon microsystems and from 2001 also on silicon microelectronics. He is presently Deputy Director of CEA-LETI in charge of European cooperation including ENIAC.

Prior to joining CEA-LETI, Brillouët worked for 23 years in Centre National des Télécommunications (CNET; France Telecom R&D Center) where he held different positions in microelectronics research, starting with interconnect developments and materials research, and moving to lithography and CMOS process integration and deputy manager of CNET's Pilot Line.

In 1992, he was assigned to the Common R&D Center between STMicroelectronics and France Télécom in Crolles, France, as Process

Development Division Manager and then Technology Director. He was in charge of all the technology R&D programs for the Crolles site, including CMOS, eDRAM and BiCMOS process and process integration.
Brillouët graduated from Ecole Polytechnique in Paris in 1974 and Telecom Paris in 1976. He has authored many technical publications and made invited talks in different conferences incl. IEDM, IITC...

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Plenary & Workshop Sessions
June 3 – 4, 2008

June 3, 2008

8:30 a.m	Opening
9:00 a.m	**Keynote : SoC in the post 45nm era**, Dr Uming Ko, TI Senior Fellow, USA

Session A	***Advanced Transistor Structure, Architecture and Process***
Co-Chairs	Don-Won Kim & Arnaud Pouydebasque
9:50 a.m	**Invited Paper: Silicon-On-Nothing (SON) Applications for Low Power Technologies**, S.Monfray, F.Boeuf, P.Coronel, G.Bidal, S.Denorme, T.Skotnicki; STMicroelectronics, France
10:00 a.m	**Invited Paper: Fully Depleted SOI devices for Low Power technologies**, O.Faynot; CEA, France
10:10 a.m	**Evaluation of Ultra Thin Body Si-On-ONO (UTB SOONO) Transistors Using Ultra Thin Spacer Technology,** Hyun Jun Bae, Sung Hwan Kim, Sung In Hong, Yong Lack Choi, Ho Ju Song , Chang Woo Oh, Dong-Won Kim, Donggun Park*, KyungSeok Oh, Won-Seong Lee; Advanced Technology Development Team 1, DPA Team*, R&D Center, Samsung Electronics Co., Korea
10:20 a.m	**New Charge Trapping Phenomena in Recessed-Channel-Array-Transistor (RCAT) after Fowler-Nordheim Stress**, Sung-Young Lee, Se Geun Park, Samjin Hwang, Jaeeun Jeon, Wonshik Lee; DRAM QA, Samsung Electronics Co., Korea
10:30 a.m	**Use of the p-floating shielding layer for improving electric field concentration of the recessed gate**, Sang Jun Hwang*, Seung Woo Yu*, Jae In Lee*, Ey-Goo Kang+, Man Young Sung*; *Department of Electrical Engineering, Korea University, Anam-Dong, Seongbuk-Gu, Seoul 136-701, Korea, +Department of Information Technology, Far East University, Uemsung-gun, Chung-buk 369-851, Korea

10:40 a.m	**Coffee Break**

Session B1	***RF & AMS***
Co-Chairs	Didier Belot
10:55 a.m	**Invited Paper: CMOS SOI technology for WPAN. Application to 60Ghz LNAs,** A. Siligaris*, C. Mounet*, B. Reig*, P. Vincent*, A. Michel+; *CEA-LETI, +ANSOFT, France
11:05 a.m	**Invited Paper: Sub-harmonic CMOS receivers at Ka-band**, F. Svelto; Pavia University, Italy
11:15 a.m	**A 0.5 V Area-Efficient Transformer Folded-Cascode Low-Noise Amplifier in 90 nm CMOS,** Takao Kihara, Hae-Ju Park, Isao Takobe, Fumiaki Yamashita, Toshimasa Matsuoka, Kenji Taniguchi; Osaka University, Japan
11:25 a.m	**A Low Power Multi-band Selector DLL with Wide-Locking Range**, Ko-Chi Kuo, Yi-Hsi Hsu; National Sun Yat-sen University, Taiwan
11:35 a.m	**Design of a Current Steering CMOS D/A Converter with an Adaptive Control Switch and a Novel Layout Technique,** Junho Moon, Sanghoon Hwang, Daeyoon Kim, Heewon Kang, Seungjin Yeo, Doobock Lee, Minkyu Song; Dongguk University, Korea

Session B2	***Low Power***
Co-Chairs	Toshinari Takayanagi & Geoffrey Yeap
10:55 a.m	**Invited Paper: 3D-Structured On-Chip Buck Converter for Distributed Power Supply System in SiPs,** Makoto Takamiya*+, Kohei Onizuka+, Takayasu Sakurai+; *VLSI Design and Education Center, University of Tokyo, Japan, +Institute of Industrial Science, University of Tokyo, Japan
11:05 a.m	**Invited Paper: A Localized Power Control Mixing Hopping and Super Cut-Off Techniques within a GALS NoC,** Edith Beigné, Fabien Clermidy, Sylvain Miermont, Yvain Thonnart,

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	Alexandre Valentian, Pascal Vivet; CEA-LETI, MINATEC, France
11:15 a.m	**Improvement of Power Supply Rejection Ratio of LDO Deteriorated by Reducing Power Consumption,** Socheat Heng, Cong-Kha Pham; Department of Electronic Engineering, the University of Electro-Communications,Tokyo, JAPAN
11:25 a.m	**An Innovative sub-32nm SRAM Current Sense Amplifier in Double-Gate CMOS Insensitive to Process Variations and Transistor Mismatch,** Adam Makosiej[*], Piotr Nasalski[*], Bastien Giraud[+], Andrei Vladimirescu[+#], Amara Amara[+]; [*]Technical University of Lodz, Poland, [+]ISEP, France, [#]Berkeley Wireless Research Center, USA
11:35 a.m	**SRAM Memory Cell Leakage Reduction Design Techniques in 65nm Low Power PD-SOI CMOS,** Olivier Thomas[*], Marc Belleville[*], Richard Ferrant[+]; [*]CEA, France– Minatec, Grenoble, France, [+]STMicroelectronics Crolles, France
11:45 a.m	**Which is the Best Dual-Port SRAM in 45-nm Process Technology? – 8T, 10T Single End, and 10T Differential –** Hiroki Noguchi[*], Shunsuke Okumura[*], Yusuke Iguchi[*], Hidehiro Fujiwara[*], Yasuhiro Morita[*], Koji Nii*[+], Hiroshi Kawaguchi[*], Masahiko Yoshimoto[*]; [*]Kobe University, Japan, [+]Renesas Technology Corporation, Japan
11:55 a.m	**Workshops A, B1, B2**
12:55 p.m	**Lunch**
Session C1	***Advanced Transistor Structure, Architecture and Process***
Co-chairs	Don-Won Kim & Arnaud Pouydebasque
2:30 p.m	**Invited Paper: Low-voltage 6T FinFET SRAM cell with high SNM using HfSiON/TiN gate stack, fin widths down to 10nm and 30nm gate length** N. Collaert[*], K. von Arnim[+], R. Rooyackers[*], T. Vandeweyer[*], A. Mercha[*], B. Parvais[*], L. Witters[*], A. Nackaerts[†], E. Altamirano Sanchez[*], M. Demand[*], A. Hikavyy[*], S. Demuynck[*], K. Devriendt[*], F. Bauer+, I. Ferain[*#], A. Veloso[*], K. De Meyer[*#], S. Biesemans[*], M. Jurczak[*]; [*]IMEC, Belgium, [+]Infineon Technologies, Germany, [#]K.U. Leuven, Belgium, [†]NXP-TSMC Research Center, Heverlee, Belgium
2:40 p.m	**Independent-Gate Four-Terminal FinFET SRAM for Drastic Leakage Current Reduction,** Kazuhiko Endo, Shin-ichi O'uchi, Yuki Ishikawa, Yongxun Liu, Takashi Matsukawa, Kunihiro Sakamoto, Meishoku Masahara, Junichi Tsukada, Kenichi Ishii, Eiichi Suzuki; National Institute of AIST, Japan
2:50 p.m	**A Study of LBO Effects in a 40 nm SA-MSCFET,** Jyi-Tsong Lin, Yi-Chuen Eng & Shiang-Shi Kang; National Sun Yat-Sen University, Taiwan
3:00 p.m	**A New Edge Termination Technique to Improve Voltage Blocking Capability and Reliability of Field Limiting Ring for Power Devices,** Yo Han Kim[*], Han Sin Lee[*], Sin su Kyung[*], Young Mok Kim[*], Ey Goo Kang[+], Man Young Sung[*]; Korea University, Korea, [+]Far East University, Korea
3:10 p.m	**An SOI-based Self-aligned Quasi-SOI MOSFET with II-shaped Semiconductor Conductive Layer,** Yi-Chuen Eng, Jyi-Tsong Lin, Shiang-Shi Kang; National Sun Yat-Sen University, Taiwan
Session C2	***Reliability***
Co-chairs	Koji Eriguchi
2:30 p.m	**Invited Paper: Reliability of Advanced Embedded Non-Volatile Memories: The 2T-FNFN Device,** Guoqiao Tao; NXP, The Netherlands
2:40 p.m	**Invited Paper: SOI Chip Design and Charging Damage,** Terence B. Hook; IBM, USA
2:50 p.m	**Invited Paper: TDDB and BTI Reliabilities of High-k Stacked Gate Dielectrics - Impact of Initial Traps in High-k Layer,** Kenji Okada[*], Hiroyuki Ota[+], Toshihide Nabatame[+], Akira

Toriumi[+#]; [*]Matsushita Electric Industrial Co., Ltd., [+]MIRAI-ASET, Japan, [#]The University of Tokyo, Japan.

3:00 p.m **Invited Paper: Reliability Issues for Nano-scale CMOS Dielectrics: - From Transistors to Product Reliability - From SiON to High-K dielectrics -**G. Ribes, M. Rafik, D. Roy, J.M. Roux; ST microelectronics, France

3:10 p.m **Threshold Voltage Shift Instability Induced by Plasma Charging Damage in MOSFETs with High-k Dielectric,** K. Eriguchi[*], M. Kamei[*], K. Okada[+], H. Ohta[*], K. Ono[*]; [*]Kyoto University, Japan, +MIRAI-ASET, Japan

3:20 p.m **Analysis of Si Substrate Damage Induced by Inductively Coupled Plasma Reactor with Various Superposed Bias Frequencies,** Y. Nakakubo, A. Matsuda, M. Kamei, H. Ohta, K. Eriguchi, K. Ono; Kyoto University, Japan

Session D1 *RF & AMS*

Co-Chairs Didier Belot

3:20 p.m **Invited Paper: Sampled Analog Signal Processing : from Software Defined to Software Radio**, Yann Deval; University of Bordeaux, France

3:30 p.m **Low-Power High Precision Integrated Nanostructure with Superior-Order Curvature-Corrected Logarithmic Core,** Cosmin Popa; UPB, Romania

3:40 p.m **Metal Gate Effects on a 32nm Metal Gate Resistor,** Thuy Dao, Ik_Sung Lim, Larry Connell, Dina H. Triyoso, Youngbog Park & Charlie Mackenzie; Freescale Semiconductor, USA

3:50 p.m **Design of a 6-bit 1GSPS Fully Folded CMOS A/D Converter For Ultra Wide Band (UWB) Applications,** Doobock Lee, Seungjin Yeo, Heewon Kang, Daeyoon Kim, Junho Moon, Minkyu Song; Dongguk University, Korea

4:00 p.m **An Integrated Class D Audio Amplifier based on Sliding Mode Control,** Remy Cellier, Gael Pillonnet, Nacer Abouchi, Monique Chiollaz; CPE Lyon/INL, France

4:10 p.m **Comparative analysis of two operational amplifier topologies for a 40MS/s 12-bit pipelined ADC in 0.35µm CMOS,** Jose-Angel Diaz-Madrid[*], Harald Neubauer[*], Gines Domenech-Asensi[+], Ramon Ruiz[+]; [*]Fraunhofer IIS ICD-A, Germany, [+]Universidad Politecnica de Cartagena, Spain

Session D2 *System Level Technology Assessment & Low Power*

Co-Chairs Philippe Royannez & Philip Christie

3:30 p.m **Invited Paper: Virtual Design for Technology Exploration - a process design integration methodology for a fabless entity - ,** Christopher Chun, Jose Corleto, Matt Nowak, Riko Radojcic; Qualcomm, USA

3:40 p.m **Invited Paper: Technology development driven by design,** Axel Nackaerts; NXP Semiconductor Belgium NV, Belgium

3:50 p.m **A low power 12-bit and 30-MS/s pipeline analog to digital converter in 0.35µm CMOS,** Fatah Rarbi[*], Daniel Dzahini[+]; [*]PSI Electronics company, [+]LPSC - IN2P3, Université Joseph Fourier,INPG, France

4:00 p.m **Sleep Circuit for SRAM Core with Improved Noise Margin,** Piyush Jain, Jitendra Dasani, Ashish Kumar; STMicroelectronics Pvt Ltd.Greater Noida, India

4:10 p.m **Low Power Clocking strategies in Deep Submicron Technologies** M. Samy Hosny[*], Yuejian Wu[+]; [*]SiliconPro Inc, Canada, [+]Nortel Networks, Canada

4:20 p.m **Energy Delay Optimization Methodology for Current-Mode Signaling for On-Chip Interconnects,** Astria Nur Irfansyah[*], Saeid Nooshabadi[+], Torsten Lehmann[*]; [*]University of New South Wales, Australia, [+]Gwangju Institute of Science and Technology, Korea

4:30 p.m **Coffee Break**

Session E *DFM/DFT/DFY/DFR*

Co-Chairs Jason Stinson & Keith Bowman

4:45 p.m **Invited Paper: Overview of DFT Features of the Sun**

	Microsystems Niagara2 CMP/CMT SPARC Chip, Tom Ziaja, Murali Gala; Sun Microsystems, USA,
4:55 p.m	**Invited Paper: Energy-Efficient and Metastability-Immune Timing-Error Detection and Recovery Circuits for Dynamic Variation Tolerance,** Keith A. Bowman, James W. Tschanz, Nam Sung Kim, Janice C. Lee, Chris B. Wilkerson, Shih-Lien L. Lu, Tanay Karnik, Vivek K. De; Intel, Hillsboro, OR, USA
5:05 p.m	**Process Variability-Induced Timing Failures — A Challenge in Nanometer CMOS Low-Power Design,** Xiaonan Zhang, Xiaoliang Bai; Qualcomm, USA
5:15 p.m	**Ring Oscillator Circuit Structures for Measurement of Isolated NBTI/PBTI Effects,**Jae-Joon Kim[*], Rahul Rao[*], Saibal Mukhopadhyay+, Ching-Te Chuang[#]; [*]IBM, Yorktown Heights, USA, [+]Georgia Institute of Technology, USA, [#]National Chiao-Tung University, Taiwan
5:25 p.m	**A Comparative Study of Variability Impact on Static Flip-Flop Timing Characteristics,** B. Rebaud[*], M. Belleville[*], C. Bernard[*], M. Robert[+], P. Maurine+, N. Azemard+; [*]CEA-LETI MINATEC, France, [+]LIRMM - CNRS - Université Montpellier II, France
5:35 p.m	**Analyzing the Effect of Process Variation to Reduce Parametric Yield Loss,** H. Ramakrishnan, S. S. Shedabale, G. Russell, A. Yakovlev; Newcastle University, UK
5:45 p.m	**Workshops C1, C2, D1, D2, E**
6:45 p.m	**End of Workshops**
8:00 p.m	**Gala dinner at Château de la Commanderie**

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8:30 a.m	**Keynote : Synergy between design and process: a key differentiator in the evolving microelectronic landscape**, Michel Brillouët; CEA-LETI Deputy Manager, France

Session F — Advanced Memory Devices

Co-Chairs	Jan Ackaert & Susumo Shuto
9:20 a.m	**Invited Paper: Low-Voltage Limitations and Challenges of Nano-Scale CMOS LSIs -A Personal View of Memory Designer-**Kiyoo Itoh; Fellow Hitachi, Japan
9:30 a.m	**Invited Paper: New writing mechanism for reliable SONOS embedded memories with thick tunnel oxide,** Michiel van Duuren, Nader Akil, Mohamed Boutchich, Dušan S. Golubović; NXP-TSMC Research Center, Belgium
9:40 a.m	**Invited Paper: Read and Write Circuit Assist Techniques for Improving Vccmin of Dense 6T SRAM Cell,** Muhammad M. Khellah, Ali Keshavarzi, Dinesh Somasekhar, Tanay Karnik, Vivek De; Circuits Research Lab, Intel Corp,USA
9:50 a.m	**Invited Paper: The Future of Flash Memory: is Floating Gate Technology Doomed to Lose The Race?** Dirk Wellekens, Jan Van Houdt; IMEC, Belgium
10:00 a.m	**SONOS Memories with Embedded Silicon Nanocrystals in Nitride by In-situ Deposition Method,** Yi-HongWu[*], Tsung-Yu Chiang[+], Sheng-Hsien Liu[*],Wen-Luh Yang[*], Tien-Sheng Chao[+], Fun-Tat Chin[*]; [*]Feng Chia University, Taichung, Taiwan, [+]National Chiao Tung University, Hsinchu, Taiwan
10:10 a.m	**Temperature-Based Phase Change Memory Model for Pulsing Scheme Assessment,** Yi-Bo Liao, Jun-Tin Lin, Meng-Hsueh Chiang; National Ilan University, Taiwan
10:20 a.m	**Ultra-high Bandwidth Memory with 3D-stacked Emerging Memory Cells,** Keiko Abe[*], Mihir P. Tendulkar[+], John R. Jameson[#], Peter B. Griffin[+], Kumiko Nomura[*], Shinobu Fujita[*], Yoshio Nishi[+]; [*]Toshiba Corporation, Japan, [+]Stanford University, USA, [#]Santa Clara University

Session G — Advanced Materials

Co-Chairs	Chadwin Young
10:30 a.m	**Invited Paper: Transconductance Enhancement of Si Nanowire Transistors By**

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Oxide-Induced Strain, A. Seike[*], T. Tange[*], I. Sano[*], Y. Sugiura[*], I. Tsuchida[*], H. Ohta[*], T. Watanabe[*], D. Kosemura[+], A. Ogura[+], I. Ohdomari[*]; [*]Waseda University, Japan, [+]Meiji University, Japan

10:40 a.m **A new analytical model for predicting SWCNT band-gap from geometrical properties** Karim El Shabrawy, Koushik Maharatna, Darren M Bagnall, Bashir M Al-Hashimi; ECS Southampton University, UK

10:50 a.m **FPGA design based Implementation of ICA algorithm for real time Blind Signal Separation,** M. Ounas[*], R.Touhami[*], S.Chitroub[*], M.C.E.Yagoub[+]; [*]USTHB University, Algeria, [+]School of Information Technology and Engineering, Canada

11:00 a.m **Probabilistic Modeling of Nanoscale Adder,** Xiaojun Lu[*], Jianping Li[*], Guowu Yang[*], Xiaoyu Song[+]; [*]University of Electronic Science and Technology, China, [+]Portland State University, Oregon, USA

11:10 a.m **A model for calculations of effective ion charges in microcircuit interconnects,** Tariel Makhviladze, Mikhail Sarychev, Yuri Zhitnikov; Institute of Physics and Technology, Russian Federation

11:20 a.m **Coffee Break**

Session H ***Soft Error Rate***

Co-Chairs Giorgio Cellere & Jean-Luc Autran

11:35 a.m **Invited Paper: Building a Reliable Internet Core Using Soft Error Prone Electronics,** Allan L. Silburt, Adrian Evans, Ana Burghelea, Shi-Jie Wen, Ron Norrish, Dean Hogle; Cisco Systems, USA

11:45 a.m **Invited Paper: Trends in DRAM Soft Error Rates and Future Testing Requirements**, C. Slayman; Sun Microsystems, USA

11:55 a.m **Real-Time Neutron and Alpha Soft-Error Rate Testing of CMOS 130nm SRAM: Altitude versus Underground Measurements,** J.L. Autran[*°], P. Roche[+], S. Sauze[*], G. Gasiot[+], D. Munteanu[*], P. Loaiza[#], M. Zampaolo[#], J. Borel[†]; [*]Aix-Marseille University, CNRS and IM2NP, France, [+]STMicroelectronics, France, [#]LSM, CEA-CNRS, France,[†]JB R&D, France, [°]University Institute of France (IUF), France, [•]ASTEP platform, France

12:05 p.m **Traces of Errors due to Single Ion in Floating Gate Memories** G.Cellere[*], A. Paccagnella[*], A. Visconti[+], M. Bonanomi[+], R. Harboe-Sørensen[#], A. Virtanen[†] ; [*]Univ. Padova, Italy, [+]STMicroelectronics, Italy, [#]European Space Agency, ESTEC, Netherlands, [†]University of Jyväskylä, Finland

12:15 p.m **Workshops F, G, H**

1:15 p.m **Lunch**

Session I ***SoC/MPSoC/SIP, IC & Platform Design & Process***

Co-Chairs Aurangzeb Khan & Dac Pham

2:20 p.m **Invited Paper: 3D Contactless Communication for IC Design,** Roberto Canegallo[*], Luca Ciccarelli[*], Federico Natali[+], Alberto Fazzi[+], Roberto Guerrieri+, Pierluigi Rolandi[*]; [*]STMicroelectronics Central CAD and Design Solutions, Italy, [+]ARCES-University of Bologna, Italy

2:30 p.m **Integration of SAW Filters,** Tarak Hdiji, Hassene Mnif, Mourad Loulou; National Engineering School of Sfax, Tunisia

2:40 p.m **Invited Paper: Dynamic Measurement of Critical-Path Timing,** Alan J. Drake[*], Robert M. Senger[*], Harmander Singh[+], Gary D. Carpenter[*], Norman K. James[*]; [*]IBM Austin Research Lab, USA [+]AMD, USA

2:50 p.m **Invited Paper: Key Considerations Given to the Design of a Next Generation Multi-core Communications Platform**, Dac Pham; Freescale Semiconductor, USA

3:00 p.m **Invited Paper: On-Chip Circuit for Measuring Jitter and Skew with Picosecond Resolution,** K. A Jenkins[*], Z. Xu[+], A.P. Jose[+], K.L. Shepard[+]; [*]IBM USA, +Columbia

University, USA

Session J	***Emerging Technology***
Co-Chairs	Simon Deleonibus & Dao Thuy
3:10 p.m	**Invited Paper: New State Variable Device Opportunities for Beyond CMOS: A System Perspective**, Victor V. Zhirnov[*], Ralph K. Cavin[*], and George I. Bourianoff[+]; [*]Semiconductor Research Corporation, USA, [+]Intel Corporation, USA
3:20 p.m	**Invited Paper: 3D Multichannels and stacked nanowires Technologies for New Design opportunities in Nanoelectronics,** T. Ernst[*], E. Bernard[*], C. Dupré[*], A. Hubert[*], S. Bécu[*], B. Guillaumot[+], O. Rozeau[*], O. Thomas[*], P. Coronel[+], J.-M. Hartmann[*], C. Vizioz[*], N. Vulliet[+], O. Faynot[*], T. Skotnicki[+], S. Deleonibus[*]; [*]CEA-LETI, Minatec, France, [+]STMicroelectronics, France
3:30 p.m	**Invited Paper: Device Architectures based on Graphene Channels,** M. Baus, T.J. Echtermeyer, B.N. Szafranek, M.C. Lemme, H. Kurz; AMO GmbH, Germany
3:40 p.m	**A simple compact model to analyze the impact of ballistic and quasi-ballistic transport on ring oscillator performance,** S. Martinie[*+], G. Le Carval[*], D. Munteanu[+], M.-A. Jaud, J.L. Autran[+#]; [*]CEA-LETI MINATEC, France, [+]IM2NP-CNRS, France, [#]Institut Universitaire de France (IUF), Paris, France.
3:50 p.m	**A 3-Tier, 3-D FD-SOI SRAM Macro,** Aamir Zia, Philip Jacob, Russell P. Kraft, John F. McDonald; Rensselaer Polytechnic Institute, USA
4:00 p.m	**3D CMOS Integration: Introduction of Dynamic coupling and Application to Compact and Robust 4T SRAM,** P.Batude[*], M.-A.Jaud[*], O.Thomas[*], L.Clavelier[*], A.Pouydebasque[*], M.Vinet[*], S.Deleonibus[*], A.Amara[+]; [*]CEA/LETI-MINATEC, France [+]ISEP, France
4:10 p.m	**Coffee Break**

Session K	***CAD***
Co-Chairs	Ruchir Puri
4:25 p.m	**A Generic Method for Variability Analysis of Nanoscale Circuits**, Saibal Mukhopadhyay; Georgia Institute of Technology, USA
4:35 p.m	**Stochastic Analysis for Crosstalk Noise of Coupled interconnects with Process Variations,** Xin Li[*], Janet M. Wang[+], Weiqing Tang[#], Huizhong Wu[*]; [*]Nanjing University of Science and Technology, China, [+]University of Arizona, USA, [#]Institute of Computing Technology of Chinese Academy of Sciences, China
4:45 p.m	**A Novel Moment-Based Methodology For Accurate And Efficient Static Timing Analysis,** Ahmed Shebaita[*], Dusan Petranovic[+], Yehea Ismail[*]; [*]Northwestern University, USA, [+]Mentor Graphics, USA
4:55 p.m	**How Does Inversed Temperature Dependence Affect Timing Sign-off**, Sean H. Wu[*+], Alexander Tetelbaum[*], Li-C. Wang[+]; [*]LSI Corporation, USA, [+]University of California Santa Barbara, USA
5:05 p.m	**Statistical Leakage Modeling in CMOS Logic Gates Considering Process Variations,** Carmelo D'Agostino[*], Philippe Flatresse[*], Edith Beigne[+], Marc Belleville[+]; [*]STMicroelectronics Crolles, FTM/DAIS, [+]CEA-LETI Grenoble, MINATEC
5:15 p.m	**Design of ST planar integrated inductors based on Infiniscale Flow,** A. Noiré[*], S. Bergeon[+], A. Olliver[*], Y. Courant[+]; [*]STMicroelectronics, France, [+]Infiniscale, France
5:25 p.m	**Workshops I, J, K**
6:25 p.m	**Closing Remarks**
6:30 p.m	**Adjourn**