Program

2010
IEEE International Conference on Integrated Circuits Design and Technology

June 2-4, 2010
Grenoble, France

Organization

Sponsorships

www.icicdt.org

Welcome

The International Conference on IC Design and Technology is the global forum for interaction and collaboration of IC design and technology for "accelerating product time-to-market". Close collaboration between multi-discipline technical fields - design/device/process - accelerates the implementation of new designs and new technologies into manufacturing.

IC industry trends toward specializing system design and manufacturing outsourcing - such as fabless design house, wafer foundry, design automation tool/software house, and semiconductor processing tool supplier - created the needs for individuals with multi-discipline technical skills for collaborations. Furthermore, advanced IC technology can no longer offer the same level of control over the many parameters that have direct adverse impact on circuit behavior. New IC designs also push the limit of technology, and in some cases require specific fine-tuning of certain process modules in manufacturing. Thus the traditionally separated communities of design and technology - design/device/process - are increasingly intertwined. Issues that require close interaction and collaboration for trade-off and optimization by all design/device/process fields are addressed in this conference. They are:

- Design/device/process optimizations and trade-off for leakage current, power consumption, & noise issues in mixed-signals, large scale IC devices, or design re-use;
- Incorporation of new materials (i.e. dual gate, multi-material active layers, etc.) in IC cell library and design of advanced transistor structures (i.e. Double Gate FDSOI, FinFET, etc.);
- Implementation of IC design and manufacturing process of new device structures (i.e. PDSOI, FDSOI, MRAM, etc.);
- Reduction of process & plasma induced damage or reduction of device/process parameter fluctuation through the optimization of circuit design & layout, device structure, manufacturing process, and semiconductor processing tool.

The International Conference on IC Design & Technology provides a forum for engineers, researchers, scientists, professors and students to cross this boundary through interactions of design and process technology on product development & manufacturing. The unique workshop style of the conference provides an opportunity to technologists and product designers to exchange breakthrough ideas and collaborate effectively. Two days of technical presentations and workshops are preceded by a one-day tutorial program of value to both the expert and the beginner.

The venue of the 2010 edition of ICICDT will be Minatec, at Parvis Louis Néel - Grenoble - France.

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Bich-Yen Nguyen, SOITEC

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Chua-Chin Wang, National Sun Yat-Sen University
Ming-Dou Ker, National Chiao Tung University

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Toshinari Takayanagi, Apple
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Chua-Chin Wang, National Sun Yat-Sen University
Geoffrey Yeap, Qualcomm

Wednesday June 2nd

9h 10h30 — **Tutorial 1 - Dr. Bernard DIENY, SPINTEC**

Spintronic: Physics, Technologies and Applications to MRAM, Mix Memory & Logic, and RF spin-oscillators

10h30-11h *Coffee break*

11h 12h30 — **Tutorial 2 - Dr. Keith Bowman - INTEL**

Mitigating the Adverse Effects of Parameter Variations on Logic Design

12h30-14h *Lunch*

14h 15h30 — **Tutorial 3 - Pr. Mitsumasa KOYANAGI, Tohoku University**

3-D Integration Technology and 3-D LSIs

15h30-16h *Coffee break*

16h 17h30 — **Tutorial 4 - Dr. Sani Nassif – IBM**

Characterization and Prediction of Technology Variability

18h-19h *Welcome reception*

Tutorial 1 - Dr. Bernard DIENY – Spintronic

Physics, Technologies and Applications to MRAM, Mix Memory & Logic, and RF spin-oscillators

Spinelectronics is a very rapidly growing area of R&D that merges magnetism and electronics. Since the discovery of GMR (Giant magnetoresistance) in 1988, several breakthroughs have further boosted this field (spin-valves 1990, tunnel magnetoresistance (TMR) 1995, spin transfer 1996). Spinelectronics has found applications in read heads of hard disk drives (1998) and more recently in non-volatile standalone memories (MRAM=Magnetic Random Access Memory). MRAMs integrate CMOS components with magnetic tunnel junctions (MTJ). MTJ consist of two magnetic layers separated by a thin oxide barrier (most often MgO, ~1nm thick). When a bias voltage is applied across this trilayer, the transparency of the barrier to electrons strongly depends on the relative orientation of magnetization in the two magnetic electrodes. This results in a change of resistance of the junction which can reach 600% at room temperature. Thanks to the non-volatility brought by the magnetic character of the electrodes, these elements are ideally suited for memory applications. Freescale launched the first MRAM product in 2006 (4Mbit chip). In this technology, the switching of the magnetization in the MRAM cell is achieved by local pulses of magnetic fields. More recently, alternative write schemes have been proposed which offer good scalability at least down to the 22nm technological node. They are based on spin-transfer writing. It was predicted in 1996 and experimentally observed for the first time in 2000 that the injection of a spin polarized current of sufficient density in a magnetic nanostructure can be used to switch the magnetization of this nanostructure. Therefore, it became possible to switch the magnetic configuration in an MTJ from parallel (low resistance state) to antiparallel (high resistance state) and vice-versa by sending bipolar pulses of current directly through the tunnel junction. The ultimate scalability of MRAM is actually expected to be achieved by a combination of spin transfer and thermally assisted switching (TA-ST-MRAM).
Beside standalone MRAM, this hybrid CMOS/MTJ technology can also find important applications in logic by allowing to intimately mix memory and logic functions (non-volatile logic). In particular, this may help reducing the power consumption of electronic systems.
Spin transfer also yields interesting perspective of application in the field of RF components. Indeed it was shown that steady magnetic excitations can be induced in magnetic tunnel junctions under DC current. This allows designing frequency tunable RF oscillators in frequency range interesting for wireless communication.

Dr Bernard DIENY graduated from Ecole Normale Supérieure de Cachan in 1981. He carried out his PhD thesis at Louis Neel laboratory in Grenoble. Dr Bernard DIENY has been conducting research in magnetism for 28 years. He has been a key actor in the pioneer work on spin-valves in 1990-1991. In 1992, he joined the “Nanostructure and Magnetism” laboratory at CEA/Grenoble where he acquired a

specialty in nanomagnetism and spinelectronics. In 2001, he co-founded “SPINTEC” in Grenoble, a public research laboratory devoted to spinelectronics and particularly hybrid CMOS/magnetic components for memories and logic applications, RF devices based on spin-transfer and ultra high density magnetic recording. Dr B.Dieny is co-inventor of 40 patents and signed more than 250 scientific publications. He received an outstanding achievement award from IBM in 1992 for the development of spin-valves. His team was finalist of the European Descartes Prize for Research for his work on thermally assisted MRAM in 2006. He was nominated CEA Research Director in 2007 and was recipient of an advanced grant from the European Research Council in 2009. He is co-founder of a start-up company “CROCUS Technology” developing Thermally Assisted and Spin Transfer MRAM.

Tutorial 2 - Dr. Keith Bowman – INTEL

Mitigating the Adverse Effects of Parameter Variations on Logic Design

Managing the impact of device and circuit parameter variations on performance and power is one of the primary challenges in microprocessor design. Parameter variations may be categorized based on the temporal scale (static and dynamic) and the spatial scale (die-to-die and within-die). Static variations are induced from fluctuations in the manufacturing process. Dynamic variations result from environmental and workload changes that occur during the microprocessor operation. Die-to-die (D2D) variations affect transistors and interconnects on a die equally. Conversely, within-die (WID) variations induce different electrical characteristics across a die. In this tutorial, the major sources of static and dynamic parameter variations, consisting of D2D and WID components, are described. Based on statistically-based models of microprocessor performance and power, the adverse effects of static variations on the performance and power distributions are elucidated. Validated with measured data, these models reveal that (i) WID variations directly impact the performance mean and the power median, and (ii) D2D variations impact the performance and power variances. Adaptive supply voltage (Vcc) and body-bias compensation circuits are presented as examples of variation-tolerant logic designs that reduce the effects of static D2D and WID variations on performance and power.
Dynamic variations further degrade the performance of conventional microprocessors by requiring a clock frequency (Fclk) guardband to ensure correct functionality within the presence of worst-case dynamic variations. Consequently, these inflexible designs cannot exploit the opportunities for higher performance by increasing Fclk or lower energy by reducing Vcc during favorable operating conditions. Since most systems usually operate at nominal conditions where worst-case scenarios rarely occur, these infrequent dynamic variations severely limit the performance and energy efficiency of conventional designs. In this tutorial, a resilient microprocessor design is presented to mitigate the Fclk guardband for dynamic variations to maximize throughput or

energy efficiency. A resilient design is a system with error-detection and error-recovery capabilities to maintain overall correct system functionality within the presence of errors. Resilient circuits enable the microprocessor to operate at an Fclk determined by nominal operating conditions. When dynamic variations induce a timing error, the error is detected and corrected to maintain proper logic functionality, thus effectively eliminating the Fclk guardband for dynamic variations. Silicon measurements from a 45nm test-chip indicate that resilient circuits enable a 41% throughput gain at equal energy or a 22% energy reduction at equal throughput, as compared to a conventional design.

Dr. Keith A. Bowman received a B.S. degree from North Carolina State University in 1994, and M.S. and Ph.D. degrees from the Georgia Institute of Technology in 1995 and 2001, respectively, all in electrical engineering. From 2001 to 2004, he worked in the Technology Computer-Aided Design (TCAD) Group at Intel Corporation, where he developed and supported statistical-based models, methodologies, and software tools to predict microprocessor performance and power variability. Since 2004, he has worked in the Circuit Research Laboratories (CRL) at Intel, where his current research focuses on the development of circuit design solutions to mitigate the impact of parameter variations on circuit performance and power.

Tutorial 3 - Pr. Mitsumasa KOYANAGI
Tohoku University

3-D Integration Technology and 3-D LSIs

In this tutorial talk, 1) 3-D integration technology, 2) 3-D hetero-integration and super-chip, 3) 3-D LSI design, and 4) Testing and dependability of 3-D LSIs are discussed. Firstly, key technologies for 3-D integration, TSV formation, microbump formation, chip or wafer stacking, are discussed. Then a super-chip integration technology for a hetero-integration is described. A number of KGDs (Known Good Dies) are simultaneously aligned and bonded onto a wafer or chips using a new self-assembly technique in the super-chip integration. Thirdly design constraints for 3-D LSIs are discussed demonstrating 3-D memory design, 3-D image sensor design, 3-D reconfigurable LSI design, and 3-D processor design. Finally test algorithm and test circuit and dependability for 3-D LSIs are discussed.

Pr. Mitsumasa Koyanagi received the B.S. degree in electrical engineering from Muroran Institute of Technology, Japan, and the M.S. and Ph.D. degrees in electronic engineering from Tohoku University, Sendai, Japan, in 1969, 1971, and 1974, respectively. In 1974, he joined the Central Research Laboratory, Hitachi, Ltd., where he worked on research and development of MOS memory device and process

technology, and invented a stacked capacitor DRAM memory cell which has been widely used in the DRAM production. Stacked capacitor DRAM was the first commercialized 3-D LSI. He employed high-k materials in DRAM for the first time in 1978. In addition, he fabricated MOS transistors with shallow junction using laser-annealing technology for the first time in 1979. From 1980 to 1985, he worked with the Device Development Center, Hitachi, Ltd. In 1985, he joined the Xerox Palo Alto Research Center, California, where he worked on research and development of submicrometer CMOS devices, poly-silicon thin-film transistors, and the design of analog/digital LSIs. In 1988, he joined the Research Center for Integrated Systems, Hiroshima University, as a Professor, where he worked on scaled MOS devices, three-dimensional (3-D) integration technology, optical interconnection, and parallel computer system specific for scientific computation. In 1992, he fabricated the smallest MOS transistor with a gate length of 70 nm. He proposed 3-D integration technology based on wafer-to-wafer bonding for the first time in 1989. Since 1994, he has been a Professor with the Department of Machine Intelligence and Systems Engineering (currently the Department of Bioengineering and Robotics), Tohoku University, where his current research interests include nano-CMOS devices, memory devices, lowvoltage and low-power integrated circuits, new intelligent memory for parallel processor systems, 3-D integration technology, optical interconnection, parallel computer system specific for scientific computation, real-time image processing systems and artificial retina chips, retinal prosthesis and brain implant devices, and brainlike computer systems. He has been researching 3-D integration technology and optical interconnection for more than 15 years. Dr. Koyanagi was awarded the 2006 IEEE Jun-ichi Nishizawa Medal, the 1996 IEEE Cledo Brunetti Award, the 2001 Award of Ministry of Education, Culture, Sports, Science and Technology, the 1994 SSDM (Solid-State Devices and Materials) Award, the 2004 Optoelectronic Technology Achievement Award (Japan Society of Applied Physics), the 1990 Okouchi Prize, etc.

Tutorial 4 - Dr. Sani Nassif – IBM

Characterization and Prediction of Technology Variability

As the semiconductor industry continues to scale silicon technology beyond the 22nm node, and in the absence of a clear alternative to silicon emerging, it becomes ever more important to understand the potential sources and magnitudes of manufacturing variability. This variability has always been important from the point of view of performance, but is projected to grow to the point where it is expected to impact correctness as well. For highly dense and regular structures like SRAM, this functionality impact is well documented and numerous device, circuit and system level responses (like supply boosting, error correcting codes, parity, and son on) have been developed to maintain SRAM yield and performance as further scaling occurs.

In this tutorial, we will review the essential sources of technology variability, show examples of how they can be characterized using special purpose test structures, as well as in-situ embedded structures. We will review some relatively recent data from 65nm and 45 nm processes which IBM has shared with researcher in several universities, and which helps show the breakdown of variability across lot, wafer, reticle, die and within die domains. We will show how the resulting characterization lends itself to representation in terms of spatial dependence, and finally close with some predictions for the future of variability down to the 12nm node.

Dr. Sani Nassif received his Bachelors degree from the American University of Beirut in 1980, and his Masters and PhD degrees from Carnegie-Mellon University in 1981 and 1985 respectively. He worked at Bell Laboratories until 1996 then joined the IBM Austin Research Laboratory where he currently manages the Silicon Analytics department, which is focused on design/technology coupling and includes activities in model to hardware matching, simulation and modelling, statistical modelling, statistical technology characterization and similar areas. He has authored numerous conference and journal publications, received several Best Paper awards (IEEE Trans. CAD, ICCAD, DAC, ISQED, SEMICON and ICCD), authored invited papers to ISSCC, IEDM, ISLPED, HOTCHIPS, and CICC, and given Keynote and Plenary presentations at Sasimi, ESSCIRC, BMAS, SISPAD, SEMICON and PATMOS. He is an IEEE Fellow (2008), a member of the IBM Academy of Technology, a member of the ACM, and has a total of 44 patents.

8h30

Opening

8h45 - 9h30

Keynote 1 - Masaki MOMODOMI - Toshiba Corporation

Future technology and application of NAND flash memory

Chair: Koji Eriguchi - Kyoto University

NAND flash market has been growing rapidly for these several years. There is even stronger demand for high capacity with affordable price for newer flash applications. But beyond 30nm technology of NAND flash memory has many difficulties. This talk will be about future device and circuit technologies including 3D-structure flash memory and its application and market analysis.

Masaki MOMODOMI has been Technology Executive of Flash Memory at Toshiba Semiconductor Company in Toshiba Corporation for 2 years. His responsibility is NAND flash and other non-volatile memory technology development. He joined the Toshiba Research and Development Center of Toshiba Corporation in 1980. Since 1987, he has been working on the circuit design and device development of NAND flash memory. Masaki MOMODOMI received the B.E degree in electronic engineering from Kyushu University, Fukuoka, Japan.

Session A: Advanced Memories

Chair: Susumu Shuto - Toshiba

9h30

Invited: High-Speed Links for Memory Interface

Jae-Yoon Sim[1], Young-Sik Kim[1], Young-Soo Sohn[2], Joo Sun Choi[2]

[1] Pohang University of Science and Technology (POSTECH)
[2] Samsung Electronics

9h40

Impact of Resistance Drift on Multilevel PCM Design

Yi-Hsuan Chiu[1], Yi-Bo Liao[2], Meng-Hsueh Chiang[1], Chia-Long Lin[1], Wei-Chou Hsu[2], Pei-Chia Chiang[3], Yen-Ya Hsu[3], Wen-Hsing Liu[3], Shyh-Shyuan Sheu[3], Keng-Li Su[3], Ming-Jer Kao[3], and Ming-Jinn Tsai[3]

[1] National Ilan University
[2] National Cheng Kung University
[3] Industrial Technology Research Institute

9h50

Dual Ferroelectric Capacitor Architecture and its Application to TAG RAM

C. Augustine, X. Fong, and K. Roy

Purdue University

10h-10h20 *Coffee break*

Session B: I/O circuits and ESD protections

Co-Chairs:
Ming-Dou Ker, National Chiao Tung Univ.
Chua-Chin Wang, National Sun Yat-Sen Univ.

10h20 **Invited: ESD challenges in advanced CMOS System on Chips**

Gernot Langguth, Christian Russ, Wolfgang Soldner, Bernhard Stein, and Harald Gossner
Infineon Technologies AG

10h30 **Invited: ESD protection for wideband RF CMOS LNAs**

D. Linten[1], S. Thijs[1] and G. Groeseneken[1,2]
[1] IMEC
[2] Katholieke Universiteit Leuven

10h40 **ESD Protection Design for Differential Low-Noise Amplifier With Cross-Coupled SCR**

Chun-Yu Lin[1], Ming-Dou Ker1[2] and Yuan-Wen Hsiao[1]
[1] National Chiao-Tung University
[2] I-Shou University

10h50 **Advanced ESD Power Clamp Design for SOI FinFET CMOS Technology**

Steven Thijs[1], David Trémouilles[2], Dimitri Linten[1], Natarajan Mahadeva Iyer[3], Alessio Griffoni[1] and Guido Groeseneken[1]
[1] IMEC
[2] LAAS/CNRS
[3] Global Foundries

11h **Comparison between isolated SCR & embedded dual isolated SCR power devices for ESD power clamp in C45 50A CMOS technology**

P. Galy, J. Bourgeat, J. Jimenez, C. Entringer A. Dray, B. Jacquier
STMicroelectronics

11h10 **New Transient Detection Circuit for Electrical Fast Transient (EFT) Protection Design in Display Panels**

Ming-Dou Ker[1], Wan-Yen Lin[1], Cheng-Cheng Yen[1], Che-Ming Yang[2], Tung-Yang Chen[2], and Shih-Fan Chen[2]
[1] I-Shou University
[2] Himax Technologies Inc.

11h20 **450 MHz 1.0 V to 1.8 V Bidirectional Mixed-Voltage I/O Buffer Using 90-nm Process**
Chua-Chin Wang, Ron-Chi Kuo, and Jen-Wei Liu
National Sun Yat-Sen University

Session C: Advanced Transistors / Materials

Co-Chairs:
Thomas Ernst – CEA LETI
Dina Triyoso - Freescale

11h30 **Invited: Fully Depleted Silicon-On-Insulator with Back Bias and strain for Low Power and High Performance applications**
F. Andrieu[1], O. Weber[1], S. Baudot2, C. Fenouillet-Béranger[1], O. Rozeau[1], J. Mazurier[1], P. Perreau[1], J. Eymery[2] and O. Faynot[1]
[1] CEA-LETI
[2] CEA INAC

11h40 **Invited: Fabrication and Electrical Characteristics of Self-aligned (SA) Gate-All-Around (GAA) Si nanowire MOSFETs (SNWFETs)**
D.-W. Kim, K. H. Yeo, S. D. Suk, M. Li, Y. Y. Yeoh, D. K. Sohn and C. Chung
Samsung Electronics

11h50 **A GPU/CUDA Implementation of the Collection-Diffusion Model to Compute**
*J.L. Autran[1], S. Uznanski[2], S. Martinie[1], P. Roche[2], G. Gasiot[2] and D. Munteanu**
[1] Aix-Marseille University and CNRS
[2] STMicroelectronics

12h00
13h00 **Workshops A, B & C**

13h00-14h00 *Lunch*

Session D: SoC & Low Power

Chair: Dac Pham - Freescale

14h00

Invited: The POWER7 Processor SOC

Dieter Wendel, Ronald Kalla, Joshua Friedrich, James Kahle, Jens Leenstra, Cedric Lichtenau, Balaram Sinharoy, William Starke and Victor Zyuban
IBM

14h10

Invited: MAGALI, a Network-on-Chip based multi-core System-on-Chip for MIMO 4G SDR

Fabien Clermidy[1], Christian Bernard[1], Romain Lemaire[1], Jérôme Martin[1], Ivan Miro-Panades[1], Yvain Thonnart[1], Pascal Vivet[1] and Norbert When[2]
[1] CEA-LETI
[2] University of Kaiserslautern

14h20

A 40nm CMOS, 1.27nJ, 330mV, 600kHz, Bose Chaudhuri Hocquenghem 252 bits frame decoder

Sylvain CLERC[1], Fady ABOUZEID[1, 2], Vincent HEINRICH[1], Abhishek JAIN[1],Andrea Mario VEGGETTI[1], Dennis CRIPPA[1], Philippe ROCHE[1], Gilles SICARD[2]
[1] STMicroelectronics
[2] TIMA Laboratory

14h30

Voltage Scaling and Body Biasing Methodology for High Performance Hardwired LDPC

Nabila MOUBDI[1,2], Philippe Maurine[2], Robin Wilson[1], Nadine Azemard[2], Sylvain Engels[1], Luis Rolindez[1], Vincent Heinrich[1]
[1] STMicroelectronics
[2] LIRMM

Session E: Reliability/Plasma Induced Damage

Co-Chairs:
Yuichiro Mitani – Toshiba
Andrea Scarpa - NXP

14h40

Invited: Pre-existing and process induced defects in high-k gate dielectrics ~Direct observation with EBIC and impact on 1/f noise~

Motoyuki Sato, Jun Chen, Takashi Sekiguchi, Toyohiro Chikyow, Jiro Yugami, Kazuto Ikeda, and Yuzuru Ohji
Toshiba

14h50	**Invited: Reliability Concerns in High-K/Metal Gate Technologies** *X. Garros[1], M. Cassé[1], G. Reimbold[1], F. Martin[1], L. Brunet[2], F. Andrieu[1] and F. Boulanger[1]* [1] CEA-LETI [2] STMicroelectronics
15h00	**Modeling the Effects of Plasma-Induced Physical Damage on Subthreshold Leakage Current in Scaled MOSFETs** *Koji Eriguchi, Masayuki Kamei, Yoshinori Takao, and Kouichi Ono* Kyoto University
15h10	**Design Solutions for Preventing Process Induced ESD Damage during Manufacturing of Interconnects** *J. Ackaert, B. Greenwood* On Semiconductor
15h20	**Power-Switch Gate-Oxide Breakdown Tolerance Techniques for Power-Gated SRAM** *Hao-I Yang, Ching-Te Chuang, and Wei Hwang* National Chiao-Tung University

15h30-15h50 *Coffee break*

Session F: 3D integration

Chair: Bich-Yen Nguyen – Soitec USA

15h50	**Invited: 3D Integration: Advantages, Enabling Technologies & Applications** *Mariam SADAKA[1], Ionut RADU[1] and Lea DI CIOCCIO[2]* [1] SOITEC [2] CEA-LETI
16h00	**Invited: Direct bonding for wafer level 3D integration** *Léa Di Cioccio[1], Ionut Radu[2], Pierric Gueguen[1] and Mariam Sadaka[2]* [1] CEA-LETI [2] SOITEC
16h10	**Through-Silicon-Via Stress 3D Modeling and Design** *Thuy Dao and Vance Adams* Freescale Semiconductor

16h20 **Progress and Challenges of Tungsten-Filled Through Silicon Via**
D.H. Triyoso, T. B. Dao, T. Kropewnicki, F. Martinez, R. Noble, and M. Hamilton
Freescale Semiconductor

Session G: CAD

Co-Chairs:
David Pan – University of Texas at Austin
Olivier Thomas – CEA LETI

16h30 **Invited: CAD for Double Patterning Lithography**
David Z. Pan[1], Jae-Seok Yang[1], Kun Yuan[1], and Minsik Cho[2]
[1] University of Texas at Austin
[2] IBM T. J. Watson Research Center

16h40 **Fast Monte Carlo Method via Reduced Sample Number and Node Filtering**
Inhak Han, Lee-eun Yu, and Youngsoo Shin
KAIST

16h50 **Computing Delay Correlations in SSTA**
Zeqin WU[1], Philippe MAURINE[1], Nadine AZEMARD[1], Gilles DUCHARME[2]
[1] LIRMM
[2] University of Montpellier II

17h10 **A Top-Down Approach for Substrate Noise Assessment Flow in Mixed-Signal and SOC Designs**
Hazem Hegazy[1], Emad Hegazi[2], Nabil Sabry[3], and Hani Ragaie[2]
[1] Mentor Graphics
[2] Ain Shams University
[3] French University in Egypt

17h10 **Overlay-Aware Interconnect Yield Modeling in Double Patterning Lithography**
Minoo Mirsaeedi and Mohab Anis
University of Waterloo

17h20 18h20 **Workshops D, E, F & G**

20h *Gala Dinner*

8h15 **Opening**

8h30

9h15

Keynote 2 - Jean-Luc JAFFARD - STMicroelectronics

Imaging market Evolution and its products & technological implications

Chair: Thuy Dao - Freescale

Imaging market has been booming over the past years mainly fuelled by the wide adoption of Imaging technologies inside mobile phone. The purpose of this presentation is to show the implication of such a quick evolution to Imaging technologies both in term of methodology and products.
The Future Evolution and its implications in term of development techniques and products will also be addressed

Jean-Luc JAFFARD graduated from Ecole Supérieure d'Electricité, France. In 1979, he joined Thomson Semiconductor (now STMicroelectronics) as mixed signal designer and has been involved in many consumer products developments such as analog TV core, remote controller, low noise VCR amplifiers, Audio and Video switches, teletext decoder. From 1990 to 1996, he was TV division design manager.
From 1996 to 1999, he initiated the Imaging activity at STMicroelectronics and contributed to the acquisition of VLSI Vision Limited. From 1999 to 2007, he had multiple activities within ST Imaging division, mainly in product development.
From 2007 to 2010, he has been Deputy General Manager of ST Imaging division and had the responsibility of the advanced technology developments for the division. He is now Business Unit Director in charge of Emerging Markets and Image Signal Processing inside ST Imaging Division

Session H: DFM/DFT/DFR/DFY

Chair: Keith Bowman - Intel

9h15

Invited: A High Resolution On-Chip Beat Frequency Detection System for Measuring BTI, HCI, and TDDB

John Keane[1,2], Xiaofei Wang[1], Devin Persaud[1], Chris H. Kim[1]
[1] University of Minnesota
[2] Intel Corporation

9h25 **Invited: Narrowing the Margins with Elastic Clocks**

Jordi Cortadella[1], Luciano Lavagnoy[2], Djavad Amiriz[3], Jonàs Casanova[1], Carlos Maciánz[3], Ferran Martorellz[3], Juan A. Moyaz[3], Luca Necchiz[3], Danil Sokolovx[4] and Emre Tuncerz[3]
[1] Universitat Politècnica de Catalunya
[2] Politecnico di Torino
[3] Elastix Corporation
[4] University of Newcastle

9h35 **Design Approach to Improve Thermo-Mechanical Reliability for High-Integrated Passive Circuits**

M. Nongaillard[1,2], B. Allard[2] and S. Jacqueline[1]
[1] IPDIA
[2] Université de Lyon

9h45 **Design of Charge Pump Circuit in Low-Voltage CMOS Process with Suppressed Return-Back Leakage Current**

Yi-Hsin Weng[1], Hui-Wen Tsai[1] and Ming-Dou Ker[1,2]
[1] National Chiao-Tung University
[2] I-Shou University

9h55-10h25 *Coffee break*

Session I: High Power/ High Voltage

Co-Chairs:
Jan Ackaert – On Semiconductors
Chua-Chin Wang, National Sun Yat-Sen Univ.

10h25 **Invited: Energy Efficient Power MOSFETs**

Marnix Tack, Jan Ackaert
On semiconductors

10h35 **A High-Efficiency DC-DC Buck Converter for Sub-3xVDD Power Supply**

Gang-Neng Sung[1], Ching-Lin Wang[1], Ping-Chang Jui[2] and Chua-Chin Wang[1]
[1] National Sun Yat-Sen University
[2] Automotive Research & Test Center (ARTC)

10h45 **Smart Power IC simulation of substrate coupled current due to majority and minority carriers transports**

Fabrizio Lo Conte, Jean-Michel Sallese and Maher Kayal
Ecole Polytechnique Fédérale de Lausanne (EPFL)

Session J: Low Power

Co-Chairs:
Geoffrey Yeap - Qualcomm
Alexandre Valentian – CEA LETI

10h55 **Invited: Emerging screen technologies impact on Application Engine IC power**
Philippe Gentric
Texas Instruments

11h05 **Invited: Low Power Technology/Circuit co-Development for Advanced Mobile Devices**
Geoffrey Yeap
Qualcomm

11h15 **Improving Efficiency of Power-Gated Circuits through Concurrent Optimization of Power Switch Size and Forward Body Biasing**
Ashoka Sathanur, Maryam Ashouei and Jos Huisken
IMEC

11h25 **A Robust Latch-Type Sense Amplifier Using Adaptive Latch Resistance**
Taejoong Song[1], Sang Min Lee[1], Jaehyouk Choi[1], Stephen Kim[1], Gyuhong Kim[2], Kyutae Lim[1] and Joy Laskar[1]
[1] Georgia Institute of Technology
[2] Samsung Electronics

11h35 **Power Switch Optimization and Sizing in 65nm PD-SOI Considering Supply Voltage Noise**
Julien Le Coz[1], Alexandre Valentian[2], Philippe Flatresse[1] and Marc Belleville[2]
[1] STMicroelectronics
[2] CEA-LETI

11h45
12h45 **Workshops H, I & J**

12h45-13h45 *Lunch*

Friday June 4th

Session K: Emerging Technologies

Chair: Simon Deleonibus – CEA LETI

13h45

Invited: Tunneling-based Devices and Circuits
L.-E. Wernersson, M. Egard, M. Ärlelid, and E. Lind
Lund University

13h55

Invited: Progress on Single Electron Transistors
Xavier Jehl, Marc Sanquer
CEA INAC

14h05

Multi Walled Carbon NanoTube Impedance
Iman Madadi, Hossein Aghababa, and Behjat Forouzandeh
University of Tehran

Session L: Soft Error Rate

Co-Chairs:
Eishi Ibe – Hitachi
Jean Luc Leray - CEA

14h15

Invited: Novel SER Standards: Backgrounds and Methodologies
Eishi Ibe, Ken-ichi Shimbo, Tadanobu Toba, Yoshio Tanuguchi and Hitoshi Taniguchi
Hitachi, Ltd.

14h25

Invited: Design techniques for soft-error mitigation
Michael Nicolaidis
TIMA Laboratory

14h35

Invited: Reflections on a SER-Aware Design Flow
Dan Alexandrescu
iRoC Technologies

14h45

Alpha-Emitter Induced Soft-Errors in CMOS 130nm SRAM: Real-Time Underground Experiment and Monte-Carlo Simulation
S. Martinie[1], S. Uznanski[2], J.L. Autran[1], P. Roche[2], G. Gasiot[2], D. Munteanu[1], S. Sauze[1], P. Loaiza[3], G. Warot[3] and M. Zampaolo[3]
[1] Aix-Marseille University and CNRS
[2] STMicroelectronics
[3] Laboratoire Souterrain de Modane

14h55

Cost Effective Soft Error Mitigation for Parallel Adders by Exploiting Inherent Redundancy
Yan Sun, Minxuan Zhang, Shaoqing Li, and Yali Zhao
National University of Defense Technology

15h05-15h25 *Coffee break*

Session M: RF, Analog & Mixed Signal

Co-Chairs:
Didier Belot – ST Microelectronics
Andrea Mazzanti – Università di Pavia

15h25

Invited: A 60GHz Receiver with 13GHz Bandwidth for Gbit/s Wireless Links in 65nm CMOS

Federico Vecchi[1,2], Stefano Bozzola[1], Massimo Pozzoni[3], Davide Guermandi[4], Enrico Temporiti[3], Matteo Repossi[3], Ugo Decanis[1], Andrea Mazzanti[1] and Francesco Svelto[1]
[1] Università degli Studi di Pavia
[2] Istituto Universitario Studi Superiori di Pavia
[3] STMicroelectronics
[4] STMicroelectronics, now with Broadcom

15h35

Invited: Dynamic Biasing Techniques for RF Power Amplifier Linearity and Efficiency Improvement

Nathalie Deltimple[1], L. Leyssenne[1], E. Kerhervé[1], Y. Deval[1] and D. Belot[2]
[1] IMS, [2] STMicroelectronics

15h45

A 6mW, 115GHz CMOS Injection-Locked Frequency Doubler with Differential Output

Enrico Monaco[1], Massimo Pozzoni[2], Francesco Svelto[3], Andrea Mazzanti[3]
[1] Università degli Studi di Modena e Reggio E. and Istituto Universitario Studi Superiori di Pavia
[2] ST Microelectronics
[3] Università degli Studi di Pavia

15h55

A low power 5 MS/s 14 bit switched capacitors Digital to Analog Converter

L. Gallin-Martel, D. Dzahini, F. Rarbi, O. Rossetto
Laboratoire de Physique Subatomique et de Cosmologie, IN2P3

16h05

A New Method for Performance Control of a Differential Active Inductor for Low Power 2.4GHz applications

François Belmas[1], Frédéric Hameau[1] and Jean-Michel Fournier[2]
[1] CEA-LETI
[2] IMEP-LHAC

16h15

Improvement of Integrated Dipole Antenna Performance Using Diamond for Intra-chip Wireless Interconnection

Xiaowei He, Jinwen Li, Minxuan Zhang, and Shubo Qi

National University of Defense Technology

16h25

Simplified Parameter Extraction Method for Modeling On-Chip Spiral Inductors

Eng Leong Tan[1] *and Wee Jin Koh*[1,2]
[1] Nanyang Technological University
[2] DSO National Laboratories

16h35 **Closing remarks**

16h50 **ICICDT 2011 Presentation**

16h50 17h50 **Workshops K, L & M**

Minatec, Parvis Louis Néel,
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