Program

2011
IEEE International Conference
on Integrated Circuits
Design and Technology

May 2-4, 2011
Kaohsiung, Taiwan

Organization

IEEE Tainan Section

Sponsorship

ASE GROUP

www.icicdt.org

ICICDT 2011

Welcome

The International Conference on IC Design and Technology is the global forum for interaction and collaboration of IC design and technology for "accelerating product time-to-market". Close collaboration of the multi-discipline technical fields - design/device/process - accelerates the implementation of new designs and new technologies into manufacturing.

IC industry trends toward specializing system design and manufacturing outsourcing - such as fabless design house, wafer foundry, design automation tool/software house, and semiconductor processing tool supplier - created the needs for individuals with multi-discipline technical skills for collaborations. Furthermore, advanced IC technology no longer can offer the same level of control over many parameters that have direct adverse impact on circuit behavior. New IC designs also push the limit of technology, and in some cases require specific fine-tuning of certain process modules in manufacturing. Thus the traditionally separated communities of design and technology - design/device/process - are increasingly intertwined. Issues that require close interaction and collaboration for trade-off and optimization by all design/device/process fields are addressed in this conference. They are:

- Design/device/process optimizations and trade-off for leakage current, power consumption, & noise issues in mixed-signals, large scale IC devices, or design re-use.
- Incorporation of new materials (i.e. dual gate, multi-material active layers, etc.) in IC cell library and design of advanced transistor structures (i.e. Double Gate FDSOI, FinFET, etc.).
- Implementation of IC design and manufacturing process of new device structures (i.e. PDSOI, FDSOI, MRAM, etc.).
- Reduction of process & plasma induced damage or reduction of device/process parameter fluctuation through the optimization of circuit design & layout, device structure, manufacturing process, and semiconductor processing tool.

As IC design & process technology continue to advance for increased performance, lower power, and accelerated time-to-market, the engineering activities, traditionally separated along the boundary of design and process technology, will have difficulties in meeting the shrinking window of product optimization tasks. The International Conference on IC Design & Technology provides a forum for engineers, researchers, scientists, professors and students to cross this boundary through interactions of design and process technology on product development & manufacturing. The unique workshop style of the conference provides an opportunity to technologists and product designers to exchange breakthrough ideas and collaborate effectively. Two days of technical presentations and workshops will be preceded by a one-day tutorial program of value to both the expert and the beginner.

The venue of 2011 ICICDT will be No.202, MingSheng 2nd Road, Kaohsiung City,Taiwan.

Committees

Organizing Committee

General Chair:
Marc Belleville, CEA-LETI

Conference Chair:
Chua-Chin Wang, National Sun Yat-Sen University

Executive Committee Chair:
Thuy Dao, Freescale Semiconductor

Secretary:
Dina H. Triyoso, Freescale Semiconductor

Local Arrangement Chairs:
Katherine Shu-Min Li, National Sun Yat-Sen University
Po-Ming Lee, National Sun Yat-Sen University
Robert Rieger, National Sun Yat-Sen University

Publication Chair:
Thomas Ea, ISEP

Publicity Chair:
Terrence Hook, IBM

Tutorial Chair:
Geoffrey Yeap, Qualcomm

Keynote & Invited Papers Chair:
Ming-Dou Ker, National Chiao-Tung University

Award Chair:
David Pan, University of Texas at Austin

Treasurer:
Soon-Jyh Chang, National Cheng Kung University

Committee

Technical Program Committee

Jan Ackaert, ON Semiconductor
Laurent Alacoque, CEA
Simone Alba, Numonyx
Ingo Aller, IBM
Himanshu Arora, Marvell Semiconductor
Marc Belleville, CEA LETI
Didier Belot, ST Microelectronics
Keith A Bowman, INTEL
Chen Hung Chang, TSMC
Ty Chen, Amazing Microelectronic Corporatin
Shui-Ming Cheng, TSMC
Kin P. Cheung, National Institute of Standard & Technology
Minsik Cho, IBM
Thuy Dao, Freescale Semiconductor
Emeric Defoucauld, CEA
Simon Deleonibus, CEA LETI
Shurong Dong, Zhejiang University
David Duarte, Intel
Koji Eriguchi, Kyoto University
Thomas Ernst, CEA
Véronique Ferlet, ESA
Phillipe Galy, STMicroelectronics
Mark Hall, Freescale
Frederic Hameau, CEA
Michael Han, Qualcomm
Hideto Hidaka, Renesas
Toshiro Hiramoto, University of Tokyo
Terrence Hook, IBM
Eishi Ibe, Hitachi
Atsuki Inoue, Fujitsu
Ben Kaczer, Imec
Rouwaida Kanj, IBM
Ming-Dou Ker, National Chiao-Tung University
Dong-Won Kim, Samsung
Yoshinori Kumura, Toshiba
Didier Lattard, CEA

Jean-Luc Leray, CEA
Dimitri Linten, IMEC
Prashant Majhi, SEMATECH
Mehrdad Manesh, Qualcomm
Andrea Mazzanti, Università di Modena e Reggio E.
Yuuichiro Mitani, Toshiba Corporation
Hiroshi Mizuta, University of Southampton UK
Dominique Morche, CEA
Bich-Yen Nguyen, SOITEC-USA
Mototsugu. Okushima, Renesas
David Pan, The University of Texas at Austin
Juergen Phlle, IBM
Ruchir Puri, IBM
Marina Reyboz, CEA
Bruno Robisson, CEA
Elyse Rosenbaum, University of Illinois at Urbana-Champaign
Philippe Royannez, TI WTBU CTC
Anne-sophie Royet, CEA
Olivier Rozeau, CEA
Ashoka Sathanur, Imec
Andrea Scarpa, NXP Semiconductors
Rich Shen, eMemory
Susumu Shuto, Toshiba Corporation
Alecandre Siligaris, CEA
Charles Slayman, Opsalacarte
Masaya Sumita, Panasonic-Matsushita
Takayanagi Toshinari, Apple
Olivier Thomas, CEA
David Trémouilles, LAAS
Dina Triyoso, Freescale Semiconductor Inc.
Jean-Chou Tseng, TSMC
Taiki Uemura, Fujitsu Semiconductor
Alexandre Valentian, CEA
Vladislav Vashchenko, Maxim
Chua-Chin Wang, National Sun Yat-Sen University
Piet Wessels, NXP
Geoffrey Yeap, Qualcomm

Monday May 2nd

9h00 10h30	**Tutorial 1 Dr. Yuanjin ZHENG, Nanyang Technological University, Singapore** Integrated RF Transceiver Circuit and System for Communication, Sensing and Biomedical Applications

10h30~11h00 *Coffee break*

11h00 12h30	**Tutorial 2 Dr. Chun-Ming HUANG - CIC** A Multi-Die Heterogeneous Integration Platform for System Prototyping

12h30~14h00 *Lunch*

14h00 15h30	**Tutorial 3 Dr. David WANG -ChipMOS TECHNOLOGIES, INC.** 3D TSV Technology Introduction -A Packaging Perspective

15h30~16h00 *Coffee break*

16h00 17h30	**Tutorial 4 Dr. Geoffrey YEAP** VLSI Technology, Qualcomm Inc. Advanced CMOS Process/Device and Circuit Co-Design for Mobile Wireless Devices

18h~20h *Tutorial Speakers & Keynote Speakers' Dinner*

Tutorials

Tutorial 1 - Dr. Yuanjin ZHENG --- Nanyang Technological University

Integrated RF Transceiver Circuit and System for Communication, Sensing and Biomedical Applications

In this tutorial, firstly, various RF transceiver architecture and key circuits are reviewed. Secondly, ultra-Wideband (UWB) impulse transceiver circuits and systems for different applications such as WPAN, WSN and WBAN are presented. Thirdly, case studies of RF transceivers for other applications like biomedical wearable sensor and implantable devices are introduced.

Yuanjin Zheng received the B.Eng. and M.Eng. degrees from Xi'an Jiaotong University, China, in 1993 and 1996, respectively, and the Ph.D. from Nanyang Technological University, Singapore, in 2001. From July 1996 to April 1998, he worked in the National Key Lab of Optical Communication Technology, University of Electronic Science and Technology of China. In 2001, he joined the Institute of Microelectronics, A*STAR, as a Senior Research Engineer, and was then promoted to a Principle Investigator. In IME, he has led and developed various projects like CMOS RF transceivers, baseband SoC for WLAN, WCDMA, ultrawideband, and low power medical radio, etc. In July 2009, he joined Nanyang Technological University as an Assistant Professor. His research interest is on GHz RFIC and SoC design, UWB system and circuits, Bio-IC system and circuits, adaptive signal and image processing algorithm and ASIC. He has published more than 70 international journal and conference papers, 11 patents filed and one book chapter (Springer). He has successfully led and contributed numerous public funded research and industry projects.

Tutorials

Tutorial 2- Dr. Chun-Ming HUANG --- CIC

MorPACK: A Multi-Die Heterogeneous Integration Platform for System Prototyping

In this talk, we will present a multi-die multi-substrate system-in-package platform for heterogeneous system integration and prototyping, namely, MorPACK (Morphing PACKage). Logically, MorPACK provides an OS-ready system design platform which includes: embedded processor(s), SDRAM, NOR Flash, peripherals, system connection fabrics, and hardware IP connector(s). Users can follow the MorPACK design guideline to design their hardware IP(s) and easily integrate the hardware IP(s) into the MorPACK design platform. Physically, the MorPACK system platform and user designed hardware IP(s) are partitioned and implemented as individual dies via same or different processes, all the fabricated dies will be packaged and assembled as a multi-substrate structure to form a single system module. We will show the MorPACK physical structure, platform architecture, connection scheme, hardware IP design flows, system integration flow, measurement results, and finally, some thermal analysis results.

Chun-Ming Huang received the B.S. degree in mathematical science from National Chengchi University, Taipei, Taiwan, R.O.C., in 1990, and the M.S. and Ph.D. degree, both in computer science, from the National Tsing-Hua University, Hsin-Chu, Taiwan, R.O.C., in 1992 and 2005, respectively. Since 1993, he has been with the National Chip Implementation Center (CIC), where he is currently a researcher and department manager in the Design Service Division (DSD). His research interests include VLSI design and testing, platform-based SOC design methodologies, system integration technologies, and multimedia communication. Dr. Huang has served as a reviewer for the Design Automation Conference (DAC), the IEEE ISCAS, the IEEE Transactions on Computers, the ACM Transactions on Design Automation of Electronic Systems (TODAES), the ACM Transactions on Embedded Computing Systems (TECS), and the Journal of Marine Science and Technology (JMST). Dr. Huang is a member of Phi Tau Phi Scholastic Honor Society.

Tutorials

Tutorial 3 - Dr. David W. WANG--- ChipMOS TECHNOLOGIES, INC.

3D TSV Technology Introduction -A Packaging Perspective

Driven by improved performance and mobile computing needs, new innovations of IC design are being explored continuously. As 3D IC using through-silicon-via (TSV) technology provides advantages in smaller form factor, lower power consumption and high level of integration, it could offer a less capital extensive alternative towards "More than Moore". By using vertical via interconnections, one may achieve wide bandwidth interconnections while significantly reduces the power consumption and package dimensions, allowing further heterogeneous integration. Thus smaller, smarter and greener devices can be more readily incorporated in variety of advanced platforms, such as: smart phone, tablet PC, MEMS, CMOS image sensor, servers etc.
In this session, subjects to be covered include a brief introduction of electronic packaging technologies evolution, future market trends and requirements, design and process requirements for interposer and 3D TSV thin-die stack used in related applications.

Dr. David W. Wang joined ChipMOS in 2007 as Vice President, Research and Strategy Development Center, ChipMOS TECHNOLOGIES, INC. one of the leading back-end assembly and test service providers for advanced memories, LCD driver semiconductors, and mixed-signal products. He is a member of SEMI Taiwan Packaging and Test Committee.
Prior to ChipMOS, he was Vice President of Fibera, Inc. a Silicon Valley startup. He served as Senior Director at Lam Research where his responsibilities included 300mm new product introduction, system automation, field escalation and management of regional teams. David also worked for IBM's Microelectronics Division for 13 years at facilities located in Endicott and East Fishkill, New York where he as Senior Engineering Manager led advanced packaging materials/process development and marketing organizations.
He was Chairman of the Board and President of Chinese American Semiconductor Professional Association (CASPA) from 2003 to 2004 and presently is a member of International Advisors. David received his Ph.D. / M.S. from the University of Michigan and B.S. from Fu Jen University. He holds 45 U.S. patents.

Tutorials

Tutorial 4 - Geoffrey YEAP--- Qualcomm Inc.

Professional Experience

VP of Technology *5/04 – present*
VLSI Technology, Qualcomm Inc.

Member, SIA International Technology Roadmap for Semiconductors (ITRS) *11/00-present*
Process Integration & Device Structures (PIDS) Technical Working Group

- Address semiconductor device scaling trends for logic and memory processes, and identify potential solutions for difficult challenges.

Sr Manager & Distinguished Member of Technical Staff, *8/00 – 5/04*
DigitalDNA Laboratories, Motorola Inc.
90nm technology node high-performance/low power/ASIC, bulk/SOI CMOS technology device design/ optimization and process integration.

Principal Staff Device Engineer, DigitalDNA Laboratories, Motorola, Inc. *4/98 -7/00*
180nm technology node low power CMOS wireless technology device design/optimization, process integration, and manufacturing.

Senior Device Technology Engineer, Technology Development Group, AMD. *7/96 - 4/98*
100nm and sub-100nm gate length high-performance CMOS device design/optimization and process integration.

Education

Ph.D., Electrical & Computer Engineering, May 1995
M.S., Electrical & Computer Engineering, December 1989
The University of Texas at Austin, Austin, Texas
B.S. with Honors, Electrical & Computer Engineering, May 1986
The University of Texas at Austin, Austin, Texas

Patents and Publications

- Over twenty US patents were granted and several pending.
- Over sixty journal and conference publications in the field of advanced semiconductor device design, simulation and modeling. Please see page 5 for detail.

Honors and Organizations

- Member, 2009 and 2010 IEDM CMOS Devices & Technology sub-committee.
- Member, 2011 VLSI Technology Symposium committee
- Member, 2002 and 2003 IEDM Integrated Circuits & Manufacturing sub-committee.
- Senior Member, IEEE (Electron Devices, Solid-State Circuits, and Circuits & Systems societies).
- Distinguished Member of Technical Staff, Motorola Inc. Engineering Technical Ladder. Motorola DigitalDNA Laboratories' On-the Spot Award for outstanding performance. Motorola Silver Quill program for promoting innovation and engineering excellence..
- Dean's Honor List, Eta Kappa Nu (National Electrical Engineering Honorary), Tau Beta Pi (National Engineering Honorary).
- Conference scholarship award by Graduate Engineering Council at The Univ. of Texas at Austin.

Tuesday May 3rd

08h30 **Opening**

08h45 **Keynote 1 - Dr. Ho-Ming TONG --- ASE Group**

09h40 **Delivering 10 - 1000x Performance**

Chair: Ming-Dou Ker, National Chiao-Tung University

Dr. Tong was elected IEEE Fellow for leadership in leading-edge integrated circuits technology and also Fellow of the Chinese Society for Management of Technology. Among the awards Dr. Tong received were the Electronics Manufacturing Technology Award from IEEE Components, Packaging and Manufacturing Technology (CPMT) Society, the John A. Wagnon Technical Achievements Award from The International Microelectronics And Packaging Society, IBM Watson Research Division Award, IBM Master Inventor, the R&D Management Innovation Award from the Ministry of Economic Affairs, Republic of China, the Outstanding Research Award of Pan Wen Yuan Foundation and seven IBM invention plateau awards. Dr. Tong received his Ph.D. degree from Columbia University in chemical engineering. He has authored/co-authored 112 patents, 100+ technical publications, as well as 2 books and 2 special journal issues on electronic packaging.

Session A: I/O Circuits and ESD Protection

Co-Chairs:
Ming-Dou Ker, National Chiao-Tung University
Dimitri Linten, IMEC

09h40 **Transient-to-Digital Converter to Detect Electrical Fast Transient (EFT) Disturbance for System Protection Design**

Cheng-Cheng Yen, Wan-Yen Lin, Ming-Dou Ker, Ching-Ling Tsai, Shih-Fan Chen, and Tung-Yang Chen

09h50 **ESD RF protections in advanced CMOS technologies and its parasitic capacitance evaluation**

Ph. Galy(1), J. Jimenez(1), Wim Schoenmaker(2), Peter Meuris(2), Olivier Dupuis(2)

(1) STMicroelectronics, 850 rue Jean Monnet, 38920 Crolles , France

(2)MAGWEL NV, Martelarenplain 13 B-3000 Leuven, Belgium

10h00 **Design of Low-Leakage Power-Rail ESD Clamp Circuit with MOM Capacitor in a 65-nm CMOS Process**

Po-Yen Chiu1 and Ming-Dou Ker1, 2

1 Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan.

2 Dept. of Electronic Engineering, I-Shou University, Kaohsiung, Taiwan.

10h10~10h30 *Coffee Break*

Tuesday May 3rd

Session B: Advanced Transistor/ Material

Chair: Dong-Won Kim, Samsung

10h30	**Invited talk 1: Title: TBD about FDSOI development for LP** Claire FENOUILLET-BERANGER; STM/Leti
10h40	**Electrical Characteristic Fluctuation of 16 nm MOSFETs Induced by Random Dopants and Interface Traps** Yung-Yueh Chiu, Fu-Hai Li, Student *Member, IEEE,* Hui-Wen Cheng,
10h50	**Invited talk 2: Excellent Silicon Thickness Uniformity on Ultra-Thin SOI for controlling Vt variation of FDSOI** Walter Schwarzenbach, Xavier Cauchy, François Boedt, Olivier Bonnin, Eric Butaud, Christophe Girard, Bich-Yen Nguyen, Carlos Mazure, Christophe Maleville
11h00	**Variability Analysis of UTBSOI Subthreshold SRAM Considering Line-EdgeRoughness, Work Function Variation and Temperature Sensitivity** Vita Pi-Ho Hu, *Student Member, IEEE*, Ming-Long Fan, *Student Member, IEEE*, Pin Su, *Member, IEEE*, and Ching-Te Chuang, *Fellow, IEEE*
11h10	**Invited talk 3: 3D Integrable Nanowire FET Sensor with Intrinsic Sensitivity Boost** Chi-On Chui, UCLA

Session C: DFM/DFT/DFR/DFY

Chair: Keith Bowman, INTEL

11h20	**Invited talk 1: Title:Timing Error Prevention using Elastic Clocking** Kwanyeob Chae, Chang-Ho Lee, and Saibal Mukhopadhyay Georgia Institute of Technology
11h30	**Time and Workload Dependent Device Variability in Circuit Simulations** D. Rodopoulos, S. Mahato, V. Valduga de Almeida Camargo, B. Kaczer, F. Catthoor, S. Cosemans, G. Groeseneken, A. Papanicolaou, D. Soudris
11h40	**Invited talk 2: Title: An On-Chip Waveform Capturer for Diagnosing Off-Chip Power Delivery** Kumpei Yoshikawa, Takushi Hashida, and Makoto Nagata Graduate School of System Informatics, Kobe University
11h50	**Interconnect Test for Core-based Designs with Known Circuit Characteristics and Test Patterns** Tung-Hua Yeh, Sying-Jyan Wang, Katherine Shu-Min Li

Tuesday May 3rd

12h00	**Invited talk 3: Title: Resilient Techniques for Low Supply Voltage Microprocessor Cache Operation** Dr. Paola Zuliani STMicroelectronics (Agrate [MI] – Italy)
12h10 13h00	**Workshop A, B&C**

13h00~14h00 *Lunch*

Session D: 3D Integration

Chair: Bich-Yen Nguyen, SOITEC-USA

14h00	**Invited talk 1: title: Special Considerations for 3DIC Circuit Design and Modeling** Sally Liu, TSMC
14h10	**A Single TSV-rail 3D Quasi Delay Insensitive Asynchronous Signaling** M. Belleville, *Senior Member, IEEE,* E. Beigne, A. Valentian
14h20	**Invited talk 2: title: Smart Stacking technology: an industrial solution for 3D layer stacking** Chrystelle Lagahe Blanchard, Soitec
14h30	**TSV Number Minimization Using Alternative Paths** Chun-Hua Cheng, Chih-Hsien Kuo, Shih-Hsu Huang Department of Electronic Engineering, Chung Yuan Christian University
14h40	**Invited talk 3: Through Silicon Via Technology using Tungsten Metallization** G. Parès, CEA-Leti

Session E: CAD

Chair: Mehrdad Manesh

14h50	**Statistical Delay Calculation with Multiple Input Simultaneous Switching** Qin Tang, Amir Zjajo, Michel Berkelaar and Nick van der Meijs
15h00	**Balanced Truncation of a Stable Non-Minimal Deep-Submicron CMOS Interconnect** Amir Zjajo, Qin Tang, Michel Berkelaar, Nick van der Meijs
15h10	**Enabling TLM-2.0 Interface on QEMU and SystemC-based Virtual Platform** Tse-Chen Yeh, Zin-Yuan Lin, and Ming-Chao Chiang Department of Computer Science and Engineering, National Sun Yat-sen University

Tuesday May 3rd

15h20	**A Fast Custom Network Topology Generation with Floorplanning for NoC-based Systems** Katherine Shu-Min Li, *Member, IEEE*, Shu-Yu Chen, *Student Member, IEEE*, Liang-Bi Chen, *Member, IEEE*, and Ruei-Ting Gu

15h30~15h50 *Coffee Break*

Session F: Advanced Memory Device

Co-Chair:
Susumu Shuto, Toshiba Corporation
Hideto Hidaka, Renesas

15h50	**Invited talk 1: title: Evolution of Embedded Flash Memory for MCU** Dr. Hideto Hidaka, Renesas Electronics Corp., JAPAN.
16h00	**Impacts of Intrinsic Device Variations on the Stability of FinFET Subthreshold SRAMs** Yin-Nien Chen, Chien-Yu Hsieh, Ming-Long Fan, Vita Pi-Ho Hu, Pin Su and Ching-Te Chuang
16h10	**Invited talk 2: title: Low-cost embedded Flash memory technology** Dr. Wein-Town Sun, eMemory Technology
16h20	**Invited talk 3: title: Phase Change Memory Technology for Low Cost Embedded Application** Dr. Paola Zuliani, STMicroelectronics (Agrate [MI] – Italy)

Session G: Reliability/Plasma Induced Damage

Co-Chairs:
Yuichiro Mitani, Toshiba Corporation
Koji Eriguchi, Kyoto University

16h30	**Invited talk 1: Topic:Crystallization Technique of Epitaxial HfO2 Thin Films on Si Substrates and their Potential for Advanced High-k Gate Stack Technology** Dr.Shinji Migita
16h40	**A New Prediction Model for Effects of Plasma-Induced Damage on Parameter Variations in Advanced LSIs** Koji Eriguchi, Yoshinori Takao, and Kouichi Ono

Tuesday May 3rd

16h50	**Invited talk 2: Impact of La on the bias-temperature instability of the Hf-based high-k n-MOSFETs** Prof. D. S. Ang, Nanyang Technological University
17h00	**Separation of NBTI Component from Channel Hot Carrier Degradation in pMOSFETs Focusing on Recovery Phenomenon** Y. Mitani, S. Fukatsu, D. Hagishima, and K. Matsuzawa
17h10 18h00	**Workshop D, E, F&G**

18h30~21h *Reception Dinner*

Wednesday May 4th

08h30 **Preparation**

08h45 **Keynote 2 - LIN, Jyh-Ming Frankwell- Andes Technology**

09h45 **Corporation**

Microprocessor IP and developing platforms that accelerate SoC time-to-market

Chair: Ming-Dou Ker, National Chiao-Tung University

With Moore's law leads IC industry to enter era of deep nano-meters, we are able to integrate much more logic gates and circuits in system-on-chip (SoC). This migration also make design of SoC becomes highly complicated. Hence the time to market becomes longer while the design cycle keeps growing. The topic of reducing design cycle, so as to accelerate SoC time to availability became critical. There are many methodologies to expedite such SoC time to market, in this presentation, methodology of using appropriate microprocessor IP and developing platforms in SoC design and development will be major tone.

Session H: High Power/High Voltage

Co-Chairs:
Jan Ackaert, ON Semiconductor
Marianne Germain, IMEC

09h45 **On the impact of the edge profile of interconnects on the occurrence of passivation cracks of plastic-encapsulated electronic power devices**

Jan Ackaert(1), Daniel Vanderstraeten(1), Bart Vandevelde (2)

(1) Corporate R&D, ON Semiconductors (2) Imec,

09h55 **Domestic Indirect Feedback Compensation of Multiple-Stage Amplifiers for Multiple-Voltage Level-Converting Amplification**

Shang-Hsien Yang and Chua-Chin Wang, Department of Electrical Engineering, National Sun Yat-Sen University

10h05~10h30 *Coffee Break*

Wednesday May 4th

Session I: Low Power

Co-Chairs:
Philippe Royannez, IME

Michael Han, Qualcomm

10h30	**Microwatt Low-noise Variable-Gain Amplifier** Chun-Yi Li, Yu-Bin Lin, Robert Rieger, Electrical Engineering Department National Sun Yat-Sen University
10h40	**Invited talk 1: SRAM Bitcell Design for Low Voltage Operation in Deep Submicron technologies** Prof Seong-Ook Jung, Yonsei University
10h50	**An Ultra-Low Power K-Band Low-Noise Amplifier Co-Designed With ESD Protection in 40-nm CMOS** Ming-Hsien Tsai1,2, Shawn S. H. Hsu1, Fu-Lung Hsueh2, Chewn-Pu Jou2, Tzu-Jin Yeh2 Ming-Hsiang Song2, and Jen-Chou Tseng2 1 Dept. of Electrical Engineering and Institute of Electronics Engineering, National Tsing Hua University, Hsinchu, Taiwan 2 Design Technology Division, Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan
11h00	**Invited talk 2: Low Power Embedded Memory Design – from System to Process Level Considerations** Esin Terzioglu, Sei Seung Yoon, ChangHo Jung, Ritu Chaba, Venu Boynapalli, Mohamed Abu-Rahma, Joseph Wang, Sam Yang, Chidi Chidambaram, Michael Han, Geoffrey Yeap, and Mehdi Sani
11h10	**65nm PD-SOI Glitch-Free Retention Flip-Flop for MTCMOS Power Switch applications** J. Le-Coz1, P. Flatresse1, S. Clerc1, M.Belleville2, A. Valentian2 1 STMicroelectronics, Crolles, France 2 CEA LETI, MINATEC campus, Grenoble, France

Wednesday May 4th

Session J: RF & Analog, Mixed signal

Co-Chairs:
Didier Belot, ST Microelectronics
Andrea Mazzanti, Università di Modena e Reggio E.

11h20	**An ultra-low energy capacitive DAC array switchingScheme for SAR ADC in biomedical applications** Chao Yuan, Yvonne Y. H. Lam School of Electrical and Electronics Engineering VIRTUS, IC Design Centre of Excellence Nanyang technological University
11h30	**Slew-Rate Controlled Output Stages for Switching DC-DC Converters** Jia-Ming Liu, Yi-Cheng Huang, Yu-Chun Ying, and Tai-Haur Kuo Department of Electrical Engineering, National Cheng Kung University
11h40	**Temperature Dependence of Device Mismatch and Harmonic Distortion in Nanoscale Uniaxial-Strained PMOSFETs** Jack J.-Y. Kuo, William P.-N. Chen, and Pin Su Department of Electronics Engineering & Institute of Electronics, National Chiao Tung University
11h50	**A 8-bit 50-Msamples/s Switched-Current Pipelined ADC with Residue Generatorand Interlaced stage** Guo-Ming Sung, *Member, IEEE* and Ying-Tzu Lai Department of Electrical Engineering, National Taipei University of Technology
12h00	**Continuously Auto-Tuned and Self-Ranged Dual- Path PLL Design with Hybrid AFC** Min Wang, Bo Zhou, Woogeun Rhee, and Zhihua Wang *Institute of Microelectronics, Tsinghua University,*
12h10 13h00	**Workshop H, I&J**

13h00~14h00 *Lunch*

Wednesday May 4th

Session K: I/O Circuits and ESD Protection

Co-Chairs:
Ming-Dou Ker, National Chiao-Tung University
Dimitri Linten, IMEC

14h00 **A Low Jitter Active Body-Biasing Control-based Output Buffer in 65nm PD-SOI**
Dimitri Soussan[1,2], Sylvain Majcherczak[1], Alexandre Valentian[2], Marc Belleville[2]
[1)] STMicroelectronics Crolles
[2)] CEA LETI, Minatec campus

14h10 **Adaptable Stimulus Driver for Epileptic Seizure Suppression**
Ming-Dou Ker1,2, Wei-Ling Chen1, and Chun-Yu Lin1
1 Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan
2 Department of Electronic Engineering, I-Shou University, Kaohsiung, Taiwan

14h20 **Gate-Driven 3.3V ESD Clamp Using 1.8V Transistors**
Guang-Cheng Wang, Chia-Hui Chen, Wen-Hsin Huang, Kuo-Ji Chen, Ming-Hsiang Song and Ta-Pen Guo, Taiwan Semiconductor Manufacturing Corp.

14h30 **Beta-Matrix ESD Network : throughout End of placement rules?**
J. Bourgeat, P. Galy, B. Jacquier

14h40 **Invited talk 1: Design of on-chip Transient Voltage Suppressor in a Silicon-based Transceiver IC to meet IEC System-Level ESD Specification**
Ryan Hsin-Chin Jiang, Tang-Kuei Tseng, Chi-Hao Chen and Che-Hao Chuang

Session L: SoC/MPSoC/SIP

Co-Chairs:
Dac Pham, Freescale Semiconductor
Masaya Sumita, Panasonic-Matsushita

14h50 **Invited talk 1: A 5.2GHz Microprocessor Chip for the IBM zEnterpriseTM System**
Dr. Huajun Wen

15h00 **An Integrated HDTV Predictive Pixel Compensator for H.264/AVC Decoder**
Ting-Chi Tong and Yun-Nan Chang
Department of Computer Science and Engineering, National Sun Yat-sen University

Wednesday May 4th

15h10	**Memoryless Bit-Serial RNS FIR Digital Filter** Wu Tao, Li Shuguo(1), and Liu Litian(2) (1) Department of Microelectronics and Nanoelectronics Tsinghua University (2) Li Shuguo and Liu Litian Institute of Microelectronics Tsinghua University
15h20	**Design of a Low-Cost Floating-Point Programmable Vertex Processor for Mobile Graphics Applications Based on Hybrid Number System** Shen-Fu Hsiao, Chan-Feng Chiu, and Chia-Sheng Wen Department of Computer Science and Engineering, National Sun Yat-Sen University

15h30~15h50 *Coffee Break*

Session M: Soft Error Rate

Chair: Eishi Ibe, Hitachi

15h50	**Invited talk1 : not confirmed yet**
16h00	**Layout Optimization to Maximize Tolerance in SEILA: Soft Error Immune Latch** Taiki Uemura, Tsunehisa Sakoda and Hideya Matsuyama
16h10	**Invited talk 2: not confirmed yet**
16h20	**Comparative Analysis of Flip-Flop designs for Soft Errors at Advanced Technology Nodes** B. L. Bhuva1, Senior Member, IEEE, K. Lilja2, Member, IEEE, J. Holts3, Member, IEEE, S.-J. Wen3, Member, IEEE, R. Wong3, Member, IEEE, S. Jagannathan, Student Member, IEEE, T. D. Loveless, Member, IEEE, M. McCurdy, Member, IEEE, Z. J. Diggins, Student Member, IEEE

Session N: Emerging Technologies

Chair: Simon Deleonibus, CEA-LETI

16h30	**Invited talk 1: Stimulated emission of near-infrared radiation from silicon quantum wells** Shinichi Saito , Hitachi
16h40	**A Frequency-Shift Readout System for FPW Allergy Biosensor** Chia-Hao Hsu, Yain-Reu Lin, Yue-Da Tsai, Yun-Chi Chen, and Chua-Chin Wang*y*, *Senior Member, IEEE* Department of Electrical Engineering, National Sun Yat-Sen University
16h50	**Invited talk 2: Scaled Nanoelectromechanical (NEM) Functional Devices** Hirsoshi Mizuta, Univ Southampton

Wednesday May 4th	
17h00	**Thresholding using Quantum-dot Cellular Automata** Anshu S Anand*, Tanumoy Adak† Department of Computer Science and Engineering National Institute of Technology, Durgapur, WB-713209, India
17h10~18h00	**Workshop K, L, M&N**