IEEE International Conference on Integrated Circuit Design and Technology

May 30th – June 1st, 2012
Austin, Texas

www.icicdt.org

ICICDT 2012

Welcome

The International Conference on IC Design and Technology is the global forum for interaction and collaboration of IC design and technology for "accelerating product time-to-market". Close collaboration of the multi-discipline technical fields - design/device/process - accelerates the implementation of new designs and new technologies into manufacturing.

IC industry trends toward specializing system design and manufacturing outsourcing - such as fabless design house, wafer foundry, design automation tool/software house, and semiconductor processing tool supplier - created the needs for individuals with multi-discipline technical skills for collaborations. Furthermore, advanced IC technology no longer can offer the same level of control over many parameters that have direct adverse impact on circuit behavior. New IC designs also push the limit of technology, and in some cases require specific fine-tuning of certain process modules in manufacturing. Thus the traditionally separated communities of design and technology - design/device/process - are increasingly intertwined. Issues that require close interaction and collaboration for trade-off and optimization by all design/device/process fields are addressed in this conference. They are:

- Design/device/process optimizations and trade-off for leakage current, power consumption, & noise issues in mixed-signals, large scale IC devices, or design re-use.
- Incorporation of new materials (i.e. dual gate, multi-material active layers, etc.) in IC cell library and design of advanced transistor structures (i.e. Double Gate FDSOI, FinFET, etc.).
- Implementation of IC design and manufacturing process of new device structures (i.e. PDSOI, FDSOI, MRAM, etc.).
- Reduction of process & plasma induced damage or reduction of device/process parameter fluctuation through the optimization of circuit design & layout, device structure, manufacturing process, and semiconductor processing tool.

As IC design & process technology continue to advance for increased performance, lower power, and accelerated time-to-market, the engineering activities, traditionally separated along the boundary of design and process technology, will have difficulties in meeting the shrinking window of product optimization tasks. The International Conference on IC Design & Technology provides a forum for engineers, researchers, scientists, professors and students to cross this boundary through interactions of design and process technology on product development & manufacturing. The unique workshop style of the conference provides an opportunity to technologists and product designers to exchange breakthrough ideas and collaborate effectively. Two days of technical presentations and workshops will be preceded by a one-day tutorial program of value to both the expert and the beginner.

The venue of 2012 ICICDT will be **at Freescale 7700 West Parmer Lane, Austin, TX 78729.**

Committees

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David Pan, Univ. of Texas
Gi-Joon Nam, IBM

DFM/DFT/DFR/DFY:
Rouwaida Kanj, IBM

Emerging Technologies:
Simon Deleonibus, CEA-LETI
Hiroshi Mizuta, University of Southampton

High Power/High Voltage:
Jan Ackaert, ON Semiconductor

3D Integration:
Bich-Yen Nguyen, SOITEC

I/O Circuits and ESD Protection:
Chua-Chin Wang, NSYSU
Philippe Galy, ST Microelectronics

Low Power:
Michael Han, Qualcomm

Reliability/Plasma-Induced Damage:
Yuichiro Mitani, Toshiba Corporation
Koji Eriguchi, Kyoto University

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Andrea Scarpa, NXP Semiconductors

SoC/MPSoC/SIP:
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Piet Wessels, NXP Semiconductors
Geoffrey Yeap, Qualcomm
Celik-Butler Zeynep, Univ. of Texas

Wednesday May 30th

9h30 10h30	**Tutorial 1 Dr. Andy Wei** **GLOBALFOUNDRIES, Malta, NY** Device Architectures Beyond the Planar CMOS Era

10h30~11h00 *Coffee break*

11h00 12h00	**Tutorial 2 Dr. Vijay Reddy** **Texas Instruments, Austin, TX** An Overview of Circuit Aging in SOCs

12h00~13h30 *Lunch*

13h30 14h30	**Tutorial 3 Prof. Chris H. Kim** **University of Minnesota, Minneapolis, MN** Circuit Techniques for Combating CMOS Reliability Effects

14h30~15h00 *Coffee break*

15h00 16h00	**Tutorial 4 Prof. Vijay Janapa Reddi** **University of Texas, Austin, TX** Hardware and Software Co-Design for Robust and Resilient Execution

Tutorials

Tutorial 1

Dr. Andy Wei – GLOBALFOUNDRIES, Malta, NY

Device Architectures Beyond the Planar CMOS Era

Planar transistor scaling has moved beyond SiOx gate oxide limits in the last decade and progressed further into this decade with the introduction of high-k and metal gates. However, further dimensional and power reduction requirements have forced a move to non-planar and/or multi-gate devices. These devices are characterized by being fully-depleted, having greatly improved electrostatics, and lower variation, but are built in non-traditional substrates and/or processes. This tutorial will review the new device architectures and discuss the new set of challenges and tradeoffs in terms of design, performance, and SoC integration.

Andy Wei received his Ph.D. from MIT in Cambridge, Mass. in 2000. Since 2000, he has worked in technology development and manufacturing at AMD in Austin and Dresden, implementing transistor performance elements into product. In 2009, AMD spun off its manufacturing division into GLOBALFOUNDRIES. Since then, Andy has been working on platform and customer-centric optimization of leading-edge technologies. Andy is currently based in Fab8, Malta, NY, with focus on next-node process architecture.

Tutorial 2

Dr. Vijay Reddy – Texas Instruments, Austin, TX

An Overview of Circuit Aging in SOCs

An overview of transistor aging is provided from a circuit and product perspective with a focus on the impact of bias temperature instability (BTI). A methodology to assess product level BTI impact will be presented along with examples of BTI circuit impact and a circuit aging silicon test characterization platform.

Vijay Reddy received the Ph.D. in Electrical Engineering from the University of Texas at Austin in 1994. He then joined Texas Instruments and has worked on transistor/circuit reliability and product qualification methodologies. He is currently a Distinguished Member Technical Staff and is the CMOS Design Reliability Manager focusing on digital, analog, and RF circuit reliability for SOC products. He has presented papers at and served on the IRPS/IEDM program committees along with invited tutorials at IRPS/ICTMS/VLSI Test Symposium. He received the 2002 & 2004 IRPS Outstanding Paper Awards and the 2002 ESD/EOS Symposium Best Paper/Best Presentation Awards. He has received fourteen patents with several pending along with more than thirty publications.

Tutorial 3

Prof. Chris H. Kim – University of Minnesota, Minneapolis, MN

Circuit Techniques for Combating CMOS Reliability Effects

In order to continue CMOS scaling towards the physical limit, care must be taken to account for each obstacle that is currently impeding our progress. The impact of Process-Voltage-Temperature (PVT) variations on circuit performance has increased with device scaling. Device aging mechanisms such as Negative Bias Temperature Instability (NBTI), Hot Carrier Injection (HCI) and Time Dependent Dielectric Breakdown (TDDB) have become serious problems undermining the long term reliability of high performance systems. In this tutorial, I will cover some of the latest research in the circuit design area for combating CMOS aging issues. Topics will range from on-chip reliability monitors and memory yield enhancement techniques to novel CAD and architecture concepts.

Chris H. Kim received his B.S. and M.S. degrees from Seoul National University and a Ph.D. degree from Purdue University. He spent a year at Intel Corporation where he performed research on variation-tolerant circuits, on-die leakage sensor design and crosstalk noise analysis. He joined the electrical and computer engineering faculty at the University of Minnesota in 2004 where he is currently an associate professor.

Prof. Kim is the recipient of an NSF CAREER Award, a Mcknight Foundation Land-Grant Professorship, a 3M Non-Tenured Faculty Award, DAC/ISSCC Student Design Contest Awards, IBM Faculty Partnership Awards, an IEEE Circuits and Systems Society Outstanding Young Author Award, ISLPED Low Power Design Contest Awards, and an Intel Ph.D. Fellowship. He is an author/coauthor of 90+ journal and conference papers and has served as a technical program committee member for a number of circuit design conferences. He was the technical program committee co-chair for the 2010 International Symposium on Low Power Electronics and Design (ISLPED) and a guest editor for the IEEE Design and Test Magazine. His research interests include digital, mixed-signal, and memory circuit design for silicon and non-silicon (organics and magnetics) technologies.

Tutorials

Tutorial 4

Prof. Vijay Janapa Reddi – University of Texas, Austin, TX

Hardware and Software Co-Design for Robust and Resilient Execution

How do we design variation-tolerant processors (and associated systems) that meet historically established high reliability standards, without exceeding fixed power budgets and finite cost constraints? This is the fundamental research challenge that present-day and future system architects face. In this tutorial, I will present how tight coupling and interaction between the hardware and software layers can enable us to overcome this challenge. In a software-assisted hardware-guaranteed cross-layer management system, the hardware is responsible for guaranteeing reliable operation (albeit suboptimally) in the event of an emergency. However, hardware-only solutions are reactive and they lack global knowledge about execution that can enable root-cause analysis to eliminate recurring emergencies. Compilers and operating systems contain such global knowledge, and they can therefore morph execution and application code on-the-fly to eliminate recurring hardware penalties, but they require hardware support. A holistic co-designed system can enable us to sustain operation at peak points without catastrophic failures, or severe fail-stop overheads. As proof-of-concept, and as an example sample point, I will present a cross-layer solution to dampen and mitigate voltage noise.

Vijay Janapa Reddi is an Assistant Professor in the Department of Electrical and Computer Engineering at The University of Texas at Austin. Prior to joining UT Austin he was a researcher at AMD Research. His interests are in the area of computer systems. He is specifically interested in applying his background and knowledge in application characterization, runtime systems and computer architecture to improve the energy-efficiency and reliability of processors. He received a Ph.D. in Computer Science from Harvard University in 2010. http://www.ece.utexas.edu/~vjreddi

Thursday May 31st

08h30 **Opening Remark – Geoffrey Yeap, Qualcomm**

08h45 09h30 **Keynote – Leon Stok – IBM's Electronic Design Automation**

Mo(o)re EDA

Chair: Chua-Chin Wang, National Sun Yat-Sen University

Electronics Design Automation is driven in a large part by Moore's law. More cores, gates, transistors and shapes require EDA tools to continue to evolve to just keep up with increasing design sizes. In addition, new developments such as 3D, Si interposers optics and require EDA tools to handle other dimensions.
But economics will continue to be the driver the next generation of electronics. With technology progress becoming drastically more expensive in all dimensions and scaling slowing down, the focus will increasingly turn to getting more out of the current technologies and more out of EDA tools. New architectures and advanced EDA tools will be crucial to the economic viability of the electronics of the future.

Leon Stok is Vice President of IBM's Electronic Design Automation group. Prior to this he held positions as director of EDA and executive assistant to IBM's Senior Vice President of Technology and Intellectual Property and executive assistant to IBM's Senior Vice President of the Technology group.
Leon Stok studied electrical engineering at Eindhoven University of Technology, the Netherlands, from which he graduated with honors in 1986. He obtained a Ph.D. degree from Eindhoven University in 1991. Leon Stok worked at IBM's Thomas J. Watson Research Center as part of the team that developed BooleDozer, the IBM logic synthesis tool. Subsequently he managed IBM's logic synthesis group and drove the development of the first physical synthesis tool: PDS, IBM's Placement Driven Synthesis tool. From 1999-2004 he directed all of IBM's design automation research as the Senior Manager Design Automation at IBM Research.
Mr. Stok has published over sixty papers on many aspects of high level, architectural and logic synthesis, low power design, placement driven synthesis and on the automatic placement and routing for schematic diagrams. He holds 6 patents in the area of EDA. He was elected an IEEE fellow for the development and application of high-level and logic synthesis algorithms.

Thursday May 31st

Session A: CAD

Chair: **David Pan, Univ. of Texas Austin**

09h30	**Invited: Design and Analysis of IC Power Delivery with On-chip Voltage Regulation**
	Peng Li
	Texas A&M University, College Station, USA
09h40	**Invited: Design Driven Patterning Optimizations for Low K1 Lithography**
	Kanak Agarwal
	IBM Austin Research Lab, Austin, USA
09h50	**Synthesis of Clock Gating Logic through Factored Form Matching**
	Inhak Han and Youngsoo Shin
	KAIST, Daejeon, Korea
10h00	**Gate Delay Modeling for Static Timing Analysis of Body-Biased Circuits**
	Dongkyu Baek, Insup Shin and Youngsoo Shin
	KAIST, Daejeon, Korea
10h10	**A New Statistical Setup and Hold Time Definition**
	Xiaoliang Bai, Prayag Patel and Xiaonan Zhang
	Qualcomm Inc., San Diego, USA

10h20~10h40 *Coffee Break*

Thursday May 31st

Session B: Reliability / PID

Chair: **K. P. Cheung, NIST**

10h40	**<u>Invited</u>: Reliability Driven Guideline for BEOL Optimization: Protecting MOS Stacks from Hydrogen-related Impurity Penetration** Ziyuan Liu(1), Fumihiko Hayashi(1), Shinji Fujieda(2), Markus Wilde(3) and Katsuyuki Fukutani(3) (1) Device & Analysis Technology Division, Renesas Electronics Corporation, Kanagawa, Japan (2) Green Innovation Research Laboratories, NEC Corporation, Ibaraki, Japan (3) Institute of Industrial Science, University of Tokyo and CREST-JST, Tokyo, Japan
10h50	**<u>Invited</u>: Superior Reliability and Reduced Time-Dependent Variability in High-Mobility SiGe Channel pMOSFETs for VLSI Logic Applications** J. Franco, B. Kaczer, J. Mitard, M. Toledano-Luque, G. Eneman, Ph. J. Roussel, M. Cho, T. Kauerauf, T. Grasser, F. Crupi, L. Witters, G. Hellings, L.-Å Ragnarsson, N. Horiguchi, M. Heyns and G. Groeseneken IMEC, Leuven, Belgium
11h00	**Optimization Problems for Plasma-Induced Damage – A Concept for Plasma-Induced Damage Design** Koji Eriguchi, Yoshinori Nakakubo, Asahiko Matsuda, Masayuki Kamei, Yoshinori Takao and Kouichi Ono Graduate School of Engineering, Kyoto University, Kyoto, Japan
11h10	**Impacts of Random Telegraph Noise on the Analog Properties of FinFET and Trigate Devices and Widlar Current Source** Chia-Hao Pao, Ming-Long Fan, Ming-Fu Tsai, Yin-Nien Chen, Vita Pi-Ho Hu, Pin Su and Ching-Te Chuang Dept. of Electronics Engineering & Institute of Electronics, National Chiao Tung University, Hsinchu ,Taiwan
11h20	**Lifetime Prediction of Channel Hot Carrier Degradation in pMOSFETs Separating NBTI Component** Y. Mitani, S. Fukatsu, D. Hagishima, and K. Matsuzawa Advanced LSI Technology Laboratory, Toshiba Corpo., Yokohama, Japan

Thursday May 31st

Session C: Low Power

Chair: Michael Han, Qualcomm

Time	Presentation
11h30	**Invited: Energy Efficient Design Techniques for a Digital Signal Processor** Paul Bassett and Martin Saint-Laurent Qualcomm Inc., Austin, USA
11h40	**BAW Filters for Ultra-Low Power Narrow-Band Applications** Carolynn Bernier and Jean-Baptiste David CEA/LETI, Minatec, Grenoble, France
11h50	**Design of Low Power, Wider Tuning Range CMOS Voltage Control Oscillator for Ultra Wideband Applications** Iji Ayobami B, Forest Zhu, and Michael Heimlich Macquarie University, Sydney, Australia
12h00	**32 nm FinFET-based 0.7-to-1.1 V Digital Voltage Sensor with 50mV Resolution** Hung Viet Nguyen and Youngmin Kim Ulsan National Institute of Science and Technology, Ulsan, Korea
12h10	**Low Power Programmable FIR Filter Using Sharing Multiplication Technique** Nahla T. Abou El Kheir(1), Moataz S. El Kharashi(1), and Magdy A. El-Moursy(2) (1) Arab Academy for Science and Technology, Alexandria, Egypt (2) Mentor Graphics Corp., Cairo, Egypt
12h20	**Single-ended Disturb-free 5T Loadless SRAM Cell using 90nm CMOS Proess** Sih-Yu Chen and Chua-Chin Wang National Sun Yat-Sen University, Kaohsiung, Taiwan

12h30 - 13h30 *Lunch*

Time	Presentation
13h30 14h30	**Workshop A & B & C**

Thursday May 31st

Session D: Emerging Technologies

Co-Chairs: **Simon Deleonibus, CEA-LETI, Grenoble, France**
Hiroshi Mizuta, University of Southampton, UK

14h30	**Invited: Low-voltage tunnel transistors: benchmarks and circuits** Akan Seabaugh, D. Jena, S. Kurtz, Y. Lu, and Q. Zhang University of Notre Dame, Notre dame, USA
14h40	**System-Level Optimization and Benchmarking of Graphene PN Junction Logic System Based on Empirical CPI Model** Chenyun Pan and Azad Naeemi Georgia Institute of Technology , Atlanta, USA
14h50	**Design of Content Addressable Memory Cell using Carbon Nanotube Field Effect Transistor** Debaprasad Das, Avishek Sinha Roy, Hafizur Rahaman, Bhargab B. Bhattacharya Bengal Engineering and Science University, Shibpur, India
15h00	**System-Level Design and Performance Modeling for Multilevel Interconnect Networks for Carbon Nanotube Field Effect Transistor** Ahmet Ceyhan and Azad Naeemi Georgia Institute of Technology , Atlanta, USA
15h10	**Invited: Nanoscale Power and Heat Management in Electronics** Andrey Y. Serov(1), Zuanyi Li(2,) Kyle L. Grosse(3), Albert D. Liao(1), David Estrada(1), Myung-Ho Bae(1), Feng Xiong(1), William P. King(2) and Eric Pop(1), (1) Dept. of Electrical & Computer Engineering, (2) Dept. of Physics, (3) Dept. of Mechanical Science & Engineering , University of Illinois, Urbana, USA

15h20 - 15h35 *Coffee Break*

Thursday May 31st

Session E: 3D Integration

Chair: **Bich-Yen Nguyen, SOITEC-USA**

Time	Presentation
15h35	**<u>Invited</u>: 3D Stacking : Where the Rubber Meets the Road** Chandra Nimmagadda, Durodami Lisk, Riko Radojcic Qualcomm, USA
15h45	**Evaluation of Non-destructive Etch Depth Measurement for Through Silicon Vias** Thuy Dao (1), Senior Member, IEEE, Tania Thomas (2), David Marx (2), and David Grant (2) (1) Freescale Semiconductor, Austin, USA; (2) Tamar Technology, Newbury Park, USA
15h55	**<u>Invited:</u> 3D Chip Package Interaction Thermomechanical Challenges: Proximity effects of Through Silicon Vias and μ–bumps** W. Guo, G. Van Der Plas, A. Ivankovic, V. Cherman, A. Mercha, M. Gonzalez, G. Eneman, Y. Civale, A. Redolfi, T. Buisson, A. Jourdan, B. Vandevelde, I. De Wolf, A. La Manna, G. Beyer, B. Swinnen, E. Beyne IMEC, Leuven, Belgium
16h05	**Analytical Modeling of Parasitics in Monolithically Integrated 3D Inverters** Joris Lacord(1,2), Perrine Batude(3), Gerard Ghibaudo(2) and Frederic Boeuf(1) (1) STMicroelectronics, Crolles, France ; (2) IMEP, Grenoble, France; (3) CEA-LETI,Grenoble, France
16h15 17h15	**Workshop D & E**

Dinner Reception 7pm at The Oasis

Friday June 1st

8h30	**Opening Remarks**

Session F: Advanced Memories

Co- Chairs: **Hideto Hidaka, Renesas Electronics Corp.**
Yoshinori Kumura, Toshiba Corp

Time	Presentation
08h45	**Invited: Phase-Change Memories for Nano-Scale Technology and Design** Fabio Pellizzer and Roberto Bez Micron Technology, Agrate Brianza, Italy
08h55	**First-ever High-Performance, Low-Power 32-bit Microcontrollers with Embedded Nanocrystal Flash and Enhanced EEPROM Memories** Jane Yater, S.-T. Kang, C. M. Hong, B. Min, D. Kolar, K. Loiko, J. Shen, B. Winstead, H. Gasquet, S. Mohammed, A. Hardell, W. Malloch, B. Cook, R. Syzdek, A. Jarrar, J. Feddeler, K. Baker, K.M. Freescale, Austin, USA
09h05	**Invited: Energy Efficiency Deterioration by Variability in SRAM and Circuit Techniques for Energy Saving without Voltage Reduction** Kawasumi, Y. Takeyama, O. Hirabayashi, K. Kushida, F. Tachibana, Y. Niki, S. Sasaki and T. Yabe Toshiba Corp., Kawasumi, Japan
09h15	**A 0.32V, 55fJ per bit access energy, CMOS 65nm bit-interleaved SRAM with radiation Soft Error tolerance** Sylvain Clerc(1), Fady Abouzeid(1), Gilles Gasiot(1), David Gauthier(2), Dimitri Soussan(1)(3), (1)STMicroelectronics, Crolles, France (2)EaSii-IC, Grenoble, France (3)CEA LETI, Grenoble, France
09h25	**Using ECC and Redundancy to minimize VMIN induced yield loss in SRAM Arrays** Guru Shamanna, Raja Gaurav, Raghavendra Y, Percy Marfatia, Bhunesh Kshatr Intel Corporation, Bangalore, India

Friday June 1st

Session G: RF & Analog, Mixed signal

Chair: **Andrea Scarpa, NXP**

09h40	**Dynamic Stage Element Matching (DSEM) in Pipeline Analog to Digital Converters (ADC)** Francis Fradette, Eric Balster, Frank Scarpino (1), Kerry Hill (2) (1) University of Dayton, Dayton, USA (2) Air Force Research Laboratory WPAFB, Ohio, USA
09h50	**Invited: Temperature and Process Compensated Clock Generator Using Feedback TPC Bias** Tzung-Je Lee (1), Doron Shmilovitz (2), Yi-Jie Hsieh, Chua-Chin Wang (3) (1) Cheng Shiu University, Kaohsiung, Taiwan (2) Tel-Aviv University, Tel-Aviv, Israel (3) National Sun Yat-Sen University, Kaohsiung, Taiwan
10h00	**Poly-Si Thin Film Transistors: Oppotunities for Low-Cost RF Applications** Kim Soo Youn,Loke Wing-Fai, Park Sang Phill, Jung Byunghoo, Roy Kaushik Purdue University, West Lafayette, USA
10h10	**Invited: Low-Power Ultra-Wide-Band Impulse Radio Transceivers for Short Range Communications** Anrea Neviani, Andrea Bevilacqua, Andrea Gerosa, Daniele Vogrig University of Padova, Padova, Italy
10h20	**A 1V, Low Power, High-Gain, 3 – 11 GHz Double-Balanced CMOS Sub-Harmonic Mixer** Rouhollah Feghhi, Sasan Naseh Ferdowsi University of Mashhad, Mashhad, Iran

Friday June 1st

Session H: Advanced Transistors / Materials

Co-Chairs: **Bich-Yen Nguyen, SOITEC**
Dong-Won Kim, Samsung

10h30	**Invited: Emerging CMOS and Beyond CMOS Technologies for ultra-low power 3D World.** CY Kang, KW Ang, R. Hill, WY Loh, J. Oh, R. Lee, D. Gilmer, G. Bersuker,. Hobbs, P. Kirsch, K. Hummler, S. Arkalgud, and R. Jammy International SEMATECH, USA
10h40	**Invited: Variability in Fully Depleted SOI devices** M. Vinet (1), T. Hook(2), Y. Le Tiec(1), R. Murphy(2), S. Ponoth(2), L. Grenouillet(1), R. Wacquez(1), (1) CAE-LET, France (2) IBM Microelectronics, Albany NY, USA
10h50	**Invited: Strained Silicon on Insulator Substrates for Fully Depleted Application** W. Schwarzenbach, N. Daval, S. Kerdilès, G. Chabanne, C. Figuet, S. Guerroudj, O. Bonnin, X. Cauchy, B.-Y. Nguyen, and C. Maleville SOITEC, France
11h00	**Robust PEALD SiN spacer for gate first high-k metal gate integration** D.H. Triyoso, V. Jaschke, J. Shu, S. Mutas, K. Hempel, J.K. Schaeffer, M. Lenski GLOBALFOUNDRIES, Germany
11h10 12h10	**Workshop F & G & H**

12h10~13h10 *Lunch*

Session I: DFM / DFT / DFR / DFY

Co-chairs: **Michael Orshansky, Univ. of Texas Austin**
Kanak Agarwal, IBM

13h10	**Invited: O(n) Layout-Coloring for Multiple-Patterning Lithography and Conflict-Removal Using Compaction** Rani S. Ghaida (1), Kanak B. Agarwal (2), Sani R. Nassif (2), Xin Yuan (3), Lars W. Liebmann (4), Puneet Gupta(1) (1) UCLA, Electrical Engineering Dept., USA (2) IBM Corp., Austin Research Lab, USA (3) IBM Corp., San Jose, USA (4) IBM Corp., Semiconductor Research & Development Center, USA

Friday June 1st

13h20	**Performance Analysis and Modeling of Deep Trench Decoupling Capacitor for 32 nm High-Performance SOI Processors and Beyond** Balaji Jayaraman (1), Sneha Gupta (1), Yanli Zhang (2), Puneet Goyal (1), Herbert Ho (2), Rishikesh Krishnan (2), Sunfei Fang (2), Sungjae Lee (3), Douglas Daley (3), Kevin McStay (2), Bernhard Wunder (3), John Barth (3), Sadanand Deshpande (1), Paul Parries (2), Rajeev Malik (2), Paul Agnello (2), Scott Stiffler (2), Subramanian S. Iyer (2) (1) IBM Corp., Semiconductor Research and Development Center, Bangalore India, (2) IBM Corp., Semiconductor Research and Development Center, Hopewell Junction, USA (3) IBM Corp., Semiconductor Research and Development Center, Essex Junction, USA
13h30	**Invited: Low-Energy Signal Processing using Circuit-Level Timing-Error Acceptance** Ku He, Andreas Gerstlauer and Michael Orshansky University of Texas, Austin, USA
13h40	**Unifying Design Data During Verification: Implementing Logic-Driven Layout Analysis and Debug** Kishore Kollu, Trey Jackson, Farhad Kharas, Anant Adke Mentor Graphics Corporation, Wilsonville, USA
13h50	**Invited: Spatial Variation Decomposition via Sparse Regression** Wangyang Zhang (1), Karthik Balakrishnan(2), Xin Li (1), Duane Boning(2), Emrah Acar(3), Frank Liu (4) and Rob Rutenbar (5) (1) Carnegie Mellon University, Pittsburgh, USA (2) Massachusetts Institute of Technology, USA (3) IBM corp., TJ Watson Lab, USA (4) IBM corp., Austin Research Lab, USA (5) University of Illinois, Urbana-Champaign, USA

14h00~14h15 *Coffee Break*

Session J: IO Circuits and ESD Protection

Co-Chairs: Philippe Galy , STMicroelectronics
Chua-Chin Wang, National Sun Yat-Sen University

14h15	**Invited: On-Chip MOS PVT Variation Monitor for Slew Rate Self-Adjusting 2×VDD Output Buffers** Chih-Lin Chen, Hsin-Yuan Tseng, Ron-Chi Kuo, and Chua-Chin Wang National Sun Yat-Sen University, Kaohsiung, Taiwan

Friday June 1st

14h25	**A Mixed LPDDR2 Impedance Calibration Technique exploiting 28nm Fully-Depleted SOI Back-Biasing** Dimitri Soussan (1,2), Alexandre Valentian (2), Sylvain Majcherczak1, Marc Belleville2 (1) STMicroelectronics, Crolles, France (2) CEA LETI, Grenoble, France
14h35	**BIMOS transistor and its applications in ESD protection in advanced CMOS technology** P. Galy, J. Jimenez, J. Bourgeat, A. Dray, G. Troussier, B. Heitz, N. Guitard, D. Marin-cudraz, H. Beckrich-Ros STMicroelectronics, Crolles, France
14h45	**High swing low capacitance ESD RF protections in advanced CMOS technologie** Jean Jimenez, Philippe Galy, Johan Bourgeat, Boris Heitz STMicroelectronics, Crolles, France

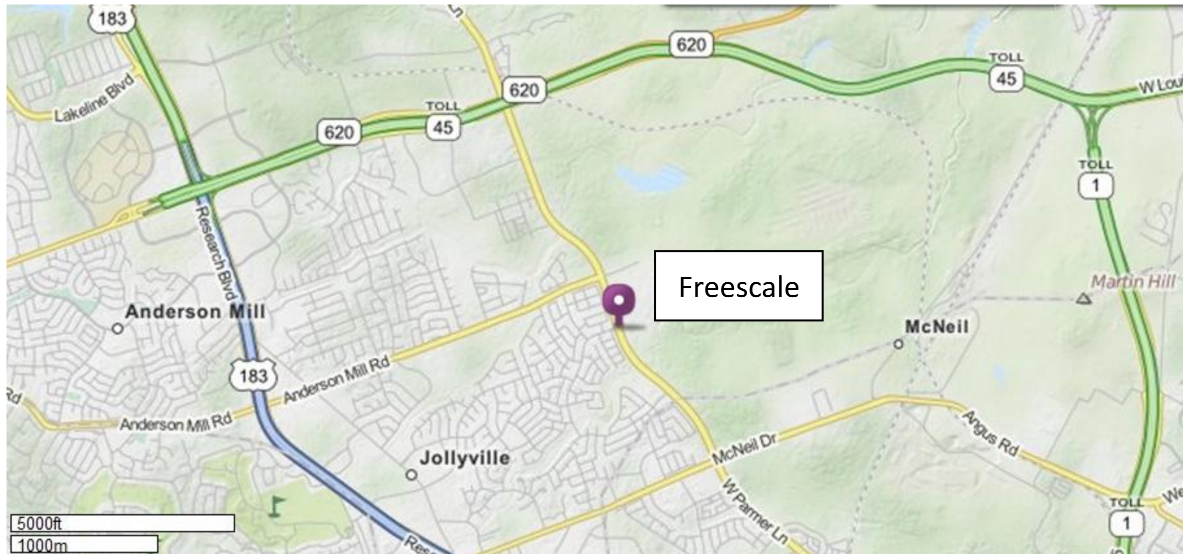
Session K: SOC / MPSoC / SIP, SER, & High-Power / High Voltage

Chair: Dac Pham, Freescale

14h55	**<u>Invited</u>: Extending Energy-Saving Voltage Scaling in Ultra Low Voltage Integrated Circuit Designs** Mingoo Seok(1), Dongsuk Jeon(2), Chaitali Chakrabati(3), David Blaauw(2), Dennis Sylvester(2) (1) Columbia University, USA (2) University of Michigan, USA (3) Arizona State University, USA
15h05	**A High Voltage Analog Multiplexer with Digital Calibration for Battery Management Systems** Chih-Lin Chen, Yi Hu, Wayne Luo, Chun-Ying Juan, Chua-Chin Wang National Sun Yat-Sen University, Kaohsiung, Taiwan
15h15	**Minimum Logic of Guaranteed Single Soft Error Resilience Based on Group Distance-Two Code** Bao Liu and Lu Wang University of Texas, San Antonio, USA

15h25	**Closing remarks**
15h35	**ICICDT 2013 Presentation**
15h45 16h45	**Workshop I & J & K**

Conference Location



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