International Conference on IC Design and Technology

May 29th- 31st, 2013
Pavia, Italy
www.icicdt.org

CONFERENCE PROGRAM

Conference Chair:	Andrea Scarpa
General Chair:	Geoffrey Yeap
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Local Arrangement Chair:	Andrea Mazzanti
Local Arrangement Responsible:	Andrea Baschirotto
Tutorial Chair:	Keith Bowman
Publication Chair:	Thomas Ea
Proceedings Responsible:	Piero Malcovati
Treasurer:	Andrea Mazzanti
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Serge Bardy, NXP
Lorenzo Cerati, ST Microelectronics
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Koji Eriguchi, Kyoto University
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Terrence Hook, IBM
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This meeting is sponsored by:

Tutorial Program

Wednesday, May 29th, 2013

9:30AM – 10:30AM: Tutorial 1

Trends in Power Semiconductors for Energy Efficient Applications

Dr. Marnix Tack, ON Semiconductors, Belgium

This tutorial will give an overview of the landscape and the trends in the field of power semiconductors, covering technologies such as power system-on-chip (SoC) "smart power," high voltage/high power discrete (both Si and wide-band-gap), and high power modules. It will be demonstrated that the main drivers for technological innovation are energy efficiency and cost at both the component and system level. This drives technology innovations for higher performance at increased switching frequency and increased integration level ("smart" systems), resulting in higher functionality at reduced footprint/weight, reduced power loss, and reduced heating at an affordable cost. Examples will be given for automotive applications, including Ecar, and computing applications.

Marnix Tack received the M.Sc. degree in electrical engineering from the University of Gent, Belgium, in 1984, and the Ph.D. degree from the Catholic University of Leuven, Belgium in 1991. He joined IMEC in 1985 working in the field of SOI-CMOS. He joined Mietec in 1990, now ON Semiconductor. He held several technical and management positions, managing programs and teams working on CMOS, SiGe-BiCMOS, NVM, BCD, and discrete power technologies. Dr. Tack is presently Senior Director of the Power Technology Centre within ON, that is developing innovative smart power and discrete high voltage and power technologies, both in Si and GaN. He (co-)authored over 70 publications and holds several patents.

10:30AM – 11:00AM: Coffee Break

11:00AM – 12:00PM: Tutorial 2

Silicon Photonics: An Industrial Perspective Enabling Low Cost Volume Applications

Dr. Guido Chiaretti, STMicroelectronics, Italy

After the first research done on the integration of photonics in silicon up to the first years of 2000, a huge work has been done worldwide with the R&D contribution of the most important industrial laboratories, like Intel, IBM, and HP for example, and many research centers. A summary of the art in this field will be given and the basic reasons of this effort will be presented and discussed. Today, Silicon Photonics is becoming a mature technology, but a lot of work has still to be done on the technological side and industrial strategy. The tutorial will also review the real advantages, some limitations, and trade-offs that a circuit designer must have clear in mind to be effective in proposing a certain solution based on Silicon Photonics. An overview of foreseen applications for which Silicon Photonics is beneficial will conclude the tutorial.

Guido Chiaretti graduated in Physics at the University of Milan, Italy in 1976. Presently, he is Director of New Technologies inside the R&D of the Imaging, Bi-CMOS ASIC & Silicon Photonics Group of STMicroelectronics located in Milan, Italy. He introduced Silicon Photonics in ST in the last seven years. He joined ST with his R&D group in 2000 bringing the Planar Lightwave Circuit (PLC) technology to develop a 32x32 optical matrix switch. From 1980 to 2000, he was the head of the Photonic Unit in the Central R&D of Italtel, where he jointly developed PLC technology with AT&T Bell Labs in early 1990's. Previously, he was also active in R&D of Optical fiber Communication, Free Space Communication, Plastic Optical Fiber Links for Automotive applications, designing many micro-optic or discrete, active or passive optical devices. From 1977 to early 1980's, he was designer of semiconductor LED and Laser sources operating in first, second, and third window on Optical Fibers.

12:00PM – 1:30PM: Lunch

1:30PM – 2:30PM: Tutorial 3

Defect-Centric Perspective of Device Reliability

Dr. Ben Kaczer, IMEC, Belgium

In the deeply downscaled CMOS devices with ~10 nm gate lengths, only a handful of defects will be present in each device, while their relative impact on the device characteristics will be significant. The defect behavior is stochastic, voltage and temperature dependent, and widely distributed in time, resulting in each device behaving very differently during operation. We will show how the physical properties of individual defects can be understood, described, and propagated to higher design abstraction levels to project device and circuit lifetime distributions.

Ben Kaczer is a Principal Scientist at IMEC, Belgium. He received the M.S. degree in Physical Electronics from Charles University, Prague, in 1992 and the M.S. and Ph.D. degrees in Physics from The Ohio State University, in 1996 and 1998, respectively. In 1998, he joined the reliability group of IMEC. He has co-authored more than 300 journal and conference papers, presented a number of invited papers and tutorials at international conferences, and received 5 IEEE IRPS Best or Outstanding Paper Awards, an IEEE IPFA Best Paper Award, and the 2011 IEEE EDS Paul Rappaport Award. He has served or is serving at various functions at the IEDM, IRPS, SISC, INFOS, and WoDiM conferences. He is currently serving on the IEEE T. Electron Dev. Editorial Board.

2:30PM – 3:00PM: Coffee Break

3:00PM – 4:00PM: Tutorial 4

From Device to Product Reliability – A Modeling Value Chain

Dr. Vincent Huard, STMicroelectronics, France

For many decades, IC component reliability relies on a top-down approach. In this approach, various elements of the product's mission profile were translated into reliability specifications at the component level. Nevertheless, this approach presents limitations in generating reliability specifications for the IPs or elementary blocks of the component. These limitations become even more important to overwhelm with the continuous technology scaling and its related increase of the reliability impact. For that purpose, lots of RnD works have been published over the last years regarding a bottom-up approach. In this approach, the reliability is dealt at design level from the beginning. In a first time, the top-down approach and its limitations will be reviewed. From that status, this tutorial will introduce the bottom-up approach and will provide the key elements (and related examples) to focus on to design and qualify products accordingly to a Design for Reliability (DFR) flow.

Vincent Huard received the B.S. (1996) in physics and the M.S. (1997) in electrical engineering from the Institut National Polytechnique de Grenoble (INPG). He worked for the CEA-Grenoble on the MBE growth of II-VI based doped heterostructures and their magneto-optical and electrical characterizations. He received his Ph.D. (2000) in physics from the University of Grenoble. In 2000 and 2001, he was a Visiting Scholar at the University of California, where he worked on devices made of ferromagnetic materials on top of semiconductors. In 2002, he joined Philips Semiconductors as a reliability engineer, working on oxide and device reliability. Since 2007, he is at STMicroelectronics, now serving as Device to Product Reliability manager, working on device and circuit reliability modeling and product qualification tests. His current research interests include NBTI, HCI and TDDB degradations both at wafer and product levels as well as design for reliability. He authored and co-authored more than 140 regular papers, several invited papers and tutorials, held 9 patents and is serving as IRPS Management Committee member.

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Conference Agenda Overview

Thursday, May 30th, 2013

Opening remarks	8:30 AM – 8:45 AM
Keynote I and Session A: CAD	8:45 AM – 10:40 AM
Coffee Break	10:40 AM – 10:55 AM
Session B: DFM/DFT/DFR/DFY	10:55 AM –12:00 PM
Session C: Low Power	12:00 PM – 12:40 PM
Lunch and Workshop A, B & C	12:40 PM – 1:40 PM
Keynote II and Session D: Advanced Transistors	1:40 PM – 3:30 PM
Coffee Break	3:15PM – 3:30 PM
Session E: Advanced Memory Devices	3:30 PM – 4:15 PM
Session F: High Power	4:15 PM – 4:55 PM
Workshop D, E &F	4:55PM – 5:55 PM
Visit to Museum and Dinner Reception	6:15 PM – 10:00 PM

Friday, May 31st, 2013

Opening remarks	8:30 AM – 8:40 AM
Session G: Emerging Technology	8:40 AM – 9:50AM
Session H: AMS	9:50 AM – 10:55 AM
Coffee Break	10:55AM – 11:10 AM
Session I: RF	11:10 AM – 12:20 PM
Lunch and Workshop G, H &I	12:20 PM – 1:20 PM
Session J: Reliability	1:20 PM – 2:05 PM
Session K: SoC /MPSoC/SIP	2:05 PM – 2:50 PM
Coffee Break	2:50 PM – 3:05 PM
Session L: 3D Integration	3:05 PM – 4:05 PM
Awards, Closing Remarks and ICICDT 2014	4:05 PM – 4:35 PM
Workshop J, K&L	4:35 PM – 5:35 PM
Post Conference Meeting for TPC	5:45 PM – 8:45 PM

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Conference Program

Thursday, May 30th, 2013

8:30 AM Welcome and opening remarks – Andrea Scarpa

Keynote: *Technology Push or Marketing Pull?*

Thursday, May 30th, 2013

8:40 AM: Introduction to Dr. Murari – Marc Belleville

8:45 AM *Keynote*- **Technology Push or Marketing Pull?** Dr. Bruno Murari, *STMicroelectronics*

Session A: CAD

Thursday, May 30th, 2013

Session Chair: David Pan and Gi-Joon Nam

9:30 AM *Invited* - **The FASTER vision for designing dynamically reconfigurable systems,** Donatella Sciuto, Marco Domenico Santambrogio, Christian Pilato, [1]Dionisios Pnevmatikatos, [1]Kyprianos Papadimitriou and [2]Dirk Stroobandt, *Polytechnic of Milano, [1]Foundation for Research and Technology Hellas, [2]Ghent University.*

9:45 AM **A Efficient Metric of Setup Time for Pulsed Flip-Flops based on Output Transition Time**, Sébastien Bernard, Alexandre Valentian, Marc Belleville, David Bol[1] and Jean-Didier Legat[1], *CEA-LETI, [1]UCL-ICTEAM.*

9:55 AM **Balanced Stochastic Truncation of Coupled 3D Interconnect**, Amir Zjajo, Nick van der Meijs and Rene van Leuken, *Delft University of Technology.*

10: 05 AM **Folded Circuit Synthesis: Logic Simplification Using Dual Edge-Triggered Flip-Flops**, Inhak Han and Youngsoo Shin, *KAIST.*

10:15 AM: *Invited* - **Exploration of Different Implementation Styles for Graphene-Based Reconfigurable Gates,** Sandeep Miryala, Andrea Calimera, Enrico Macii and Massimo Poncino, *Politecnico di Torino.*

10:30 AM: **Modeling of isolated EDMOS in advanced CMOS technologies,** Antoine Litty, Sylvie Ortolland, Sorin Cristoloveanu[1], Helene Beckrich Ros, and Dominique Golanski, *STMicroelectronics, [1]IMEP-INP.*

10:40 AM: Coffee Break

Session B – DFM/DFT/DFR/DFY

Thursday, May 30th, 2013

Session Chair: Rouwaida Kanj

10:55 AM: *Invited* - **Evaluating the Accuracy of SRAM Margin Simulation Through Large Scale Monte-Carlo Simulations with Accurate Compact Models,** Plamen Asenov, Campbell Millar[1], Scott Roy[2], Dave Reid[1], Dave New and Asen Asenov[2], *ARM, Gold Standard Simulations Ltd., [2]University of Glasgow.*

11:10 PM: **Convolution/Deconvolution SRAM Analyses for Complex Gamma Mixtures RTN Distributions**, Worawit Sohma and Hiroyuki Yamauchi, *Fukuoka Institute of Technology.*

11:20 AM: *Invited* **- Accelerated Reliability Testing of Flash Memory,** Marcello Calabrese, Carmine Miccoli[1], Christian Monzio Compagnoni[1], Luca Chiavarone, Silvia Beltrami, Andrea Parisi, Sebastiano Bartolone, Andrea Lacaita[1], Alessandro Spinelli[1], and Angelo Visconti, *Micron Semiconductor Italy,[1] Politecnico di Milano.*

11:35 PM: **Evaluating analog circuit performance in light of MOSFET aging at different time scales**, Husni Habal and Helmut Graeb, *Technical University Munich.*

11:45 PM: *Invited* - **Process variation-tolerant 3D microprocessor design: an efficient architectural solution,** Joonho Kong and Sung Woo Chung[1], *Rice University, [1]Korea University.*

Session C – Low Power

Thursday, May 30th, 2013

Session Chair: Michael Han

12:00 PM: *Invited* - **Challenges of Operating 3D Devices at Very Low Voltage,** S. Banna, *GLOBALFOUNDRIES.*

12:15 PM: **Optimization of a Voltage Sense Amplifier operating in Ultra Wide Voltage Range with Back Bias Design Techniques in 28nm UTBB FD-SOI Technology**, Guillaume Moritz, Jean-Philippe Noel[1], Bastien Giraud, Anuj Grover[1] and David Turgis[1], *CEA-LETI, [1]STMicroelectronics.*

12:25 PM: **A capacitively coupled clock distribution network with correction for process dependent skew**, Dyuthi Kishan, Maryam Shojaei Baghini and Dinesh K. Sharma, *IIT Bombay, India.*

12:35 PM-1:35PM: Lunch Buffet and Workshop Sessions A, B & C

Keynote: *Complex Trade-offs - Enablement of Moore and More than Moore*

Thursday, May 30th, 2013

1:40 PM: Introduction to Dr. Wristers – Marc Belleville

1:45 PM: *Keynote* - **Complex Trade-offs - Enablement of Moore and More than Moore,** Dr. Dirk Wristers, VP Technology and R&D, *GLOBALFOUNDRIES.*

Session D: Advanced Transistors

Thursday, May 30th, 2013

Session Chair: Bich-Yen Nguyen, Akif Sultan

2:35 PM: **Impacts of Single Trap Induced Random Telegraph Noise on Si and Ge Nanowire FETs, 6T SRAM Cells and Logic Circuits**, Shao-Yu Yang, Yin-Nien Chen, Ming-Long Fan, Pi-Ho Hu, Pin Su and Ching-Te Chuang, *National Chiao Tung University, Hsinchu Taiwan.*

2:45 PM: **Channel Length of MOSFET with Halo**, Kazuo Terada, Kazuhiko Sanai, Shouhei Matsuoka and Katsuhiro Tsuji, *Hiroshima City University.*

2:55 PM: **Impact of precursors choice on characteristics of PEALD SiN for spacer applications**, Dina Triyoso, Klaus Hempel, Susanne Ohsiek, Jeff Shu, Jamie Schaeffer and Markus Lenski, *GLOBALFOUNDRIES.*

3:05 PM: **Quantum Confinement Effect in Strained-$Si_{1-x}Ge_x$ Double-Gate Tunnel Field-Effect Transistors,** Nguyen Dang Chien, Chun-Hsing Shih, Luu The Vinh[1] and Nguyen Van Kien, *National Chi Nan University, [1] Industrial University of Ho Chi Minh City.*

3:15 PM: Coffee Break

Session E – Advanced Memory Devices

Thursday, May 30th, 2013

Session Chair: Hideto Hidaka

3:30 PM *Invited* - **Status and Perspectives of embedded Non-Volatile Memories,** Alfonso Maurelli, *STMicroelectronics.*

3:45 PM **CBRAM-based Compact Interconnect Switch for Non-volatile Reconfigurable Logic Circuits**, Santosh Onkaraiah, Marc Belleville, Marina Reyboz, Fabien Clermidy, Elisa Vianello, Jean Michel Portal[1] and Christophe Muller[1], *CEA LETI, [1] Aix-Marseille University.*

3:55 PM **A Compact Model of Hafnium-Oxide-Based Resistive Random Access Memory,** Francesco Maria Puglisi, Paolo Pavan, Andrea Padovani and Luca Larcher, *University of Modena and Reggio Emilia.*

4:05 PM **6T SRAM performance and power gain using Double Gate MOS in 28nm FDSOI Technology**, Vivek Asthana, Malathi Kar, Jean Jimenez, Sebastien Haendler and Philippe Galy, *STMicroelectronics.*

Session F – High Power

Thursday, May 30th, 2013

Session Chair: Jan Ackaert

4:15 PM **Impact of the leadframe profile on the occurrence of passivation cracks of plastic-encapsulated electronic power devices,** Jan Ackaert, Aditi Mallik and Daniel Vanderstraeten, *On semiconductors.*

4:25 PM **High Voltage Operational Amplifier and High Voltage Transceiver Using 0.25 um 60V BCD Process for Battery Management Systems,** Chih-Lin Chen, Yi-Lun Wu, Chun-Ying Juan[1] and Chua-Chin Wang, *National Sun Yat Sen University, [1]MIRDC.*

4:35 PM **Improved Deep Trench Isolation Breakdown Voltage for SmartMOS,** Thuy Dao, Todd Roggenbauer and Gordon Boyd, *Freescale.*

4:45 PM **High-Voltage Integrated Class-B Amplifier for Ultrasound Transducers** Dario Bianchi, Fabio Quaglia[1] and Andrea Mazzanti, *Università degli Studi di Pavia, [1]STMicroelectronics.*

4:55 PM – 5:55 PM: Workshop Sessions D, E & F

6:15 PM: Visit to University Museum

8:00 PM: Dinner Reception

Friday, May 31st, 2013

8:30 AM Opening remarks

Session G – Emerging Technology

Friday, May 31st, 2013

Session Chair: Simon Deleonibus

8:40 AM *Invited* - **Silicon-based Quantum Computation,** Stephanie Simmons, *Oxford University.*

8:55 AM **Dual-gate junction-less FET-detection for in-plane nano-electro-mechanical resonators,** Faezeh Arab Hassani, Hiroshi Mizuta, Yoshishige Tsuchiya[1], Cecilia Dupré[2], Eric Ollier[2], Sebastian T Bartsch[3] and Adrian Mihai Ionescu[3], *Japan Advanced Institute of Science and Technology, [1]University of Southampton, [2]CEA-LETI, [3]EPFL.*

9:05 AM: **Automatic Trimming Procedure to Enhance the Accuracy of On-chip Analog Pulse Generators,** Erika Covi, Alessandro Cabrini and Guido Torelli, *University of Pavia.*

9:15 AM: *Invited* **- Analog to Digital Converters on Plastic Foils,** Sahel Abdinia, Daniele Raiteri, Stephanie Jacob[1], Romain Coppard[1], Pieter van Lieshout[2], Giuseppe Palmisano[3], Antonino Scuderi[4], Arthur van Roermund and Eugenio Cantatore, *Eindhoven University of Technology ,[1] CEA-LIten ,[2]Polymer Vision,[3] University of Catania, [4]STMicroelectronics.*

9:30 AM: **High-Swing Buffer for Programmable Resistive Memories,** Erika Covi, Alessandro Cabrini and Guido Torelli, *University of Pavia.*

9:40 AM: **Biosequences analysis on NanoMagnet Logic,** Juan Chi Wang, Marco Vacca, Mariagrazia Graziano, Massimo Ruo Roch and Maurizio Zamboni, *Polytechnic of Torino.*

Session H - AMS

Friday, May 31st, 2013

Session Chair: Stefano D'Amico and Serge Bardy

9:50 AM *Invited* - **Towards Minimum Power Analog Filters,** Stefano D'Amico, Marcello De Matteis[1] and Andrea Baschirotto[1], *University of Salento, [1]University of Milano Bicocca.*

10:05 AM **32 Channel 12 bit Single Slope A/D Converter for LHC environment**, Marcello De Matteis, Tommaso Vergine, Stefano D'Amico, Kostas Kloukinas, Alessandro Marchioro, Andrea Baschirotto and Vincenzo Chironi, *University of Milano Bicocca.*

10:15AM **A 14 bit Extended Range Incremental DELTA-SIGMA DC for Biomedical application,** Marcello De Matteis, Domenico Cavallo, Marco Ronchi, Elio Guidetti, Giuseppina Leggeri and Andrea Baschirotto, *University of Milano Bicocca.*

10:25 AM **A Low-Power CMOS 0.13 µm Charge-Sensitive Preamplifier for GEM Detectors**, Marcello De Matteis, *University of Milano Bicocca.*

10:35 AM **Design of High-Order Class-D Audio Amplifiers**, Davide Cartasegna, Piero Malcovati, Lorenzo Crespi, Kyehyung Lee and Andrea Baschirotto, *Conexant Systems.*

10:45 AM **A 10Bit, 10MS/s, Low Power Cyclic ADC**, Wei-Zen Chen and Chien-Hung Chen, *National Chiao-Tung University.*

10:55 AM: Coffee Break

Session I - RF

Friday, May 31st, 2013

Session Chair: Stefano D'Amico and Serge Bardy

11:10 AM **A Reconfigurable Passive Mixer for Multi-Standard Receivers in 0.18 um CMOS,** Kuan Bao, Xiangning Fan and Zhigong Wang, *Southeast University.*

11:20 AM: **A 34µW 75dB-Dynamic-Range CMOS Analog Front-End for Intelligent Tire Sensor Network,** Marcello De Matteis, Tommaso Vergine, Marco Sabatini and Andrea Baschirotto, *University of Milano Bicocca.*

11:30 AM: **Breast Cancer Detection based on an UWB Imaging System: Receiver Design and Simulations,** Xiaolu Guo, Mario R. Casu, Mariagrazia Graziano and Maurizio Zamboni, *Polytechnic of Torino*.

11:40 AM: **A Dual-Band Balun LNA Resilent to 5-6 GHz WLAN Blockers for IR-UWB in 65nm CMOS**, Vincenzo Chironi, Stefano D'Amico, Andrea Baschirotto and Marcello De Matteis, *University of Milano Bicocca.*

11:50 AM: **Design and Modeling of Passive Mixer-First Receivers for Broadband Millimeter-Wave Applications,** Anna Moroni and Danilo Manstretta, *University of Milano Bicocca.*

12:00 PM: **Noise Optimization of a Broadband LNA for Tuner Applications,** Hasan Gul and Alexander Simin, *NXP Semiconductors.*

12:10 PM: **Characterization and Modeling of Depletion-Type nMOS Transistors for RF Switches with Zero Power Consumption in ON-State,** Cristian Andrei, Guy Imbert and Andrea Scarpa, *NXP Semiconductors.*

12:20PM-1:20PM: Lunch Buffet and Workshop Sessions G, H & I

Session J - Reliability

Friday, May 31st, 2013

Session Chair: Koji Eriguchi

1:20 PM: *Invited* - **High-Speed and Highly Accurate Evaluation of Electrical Characteristics in MOSFETs,** Akinobu Teramoto, Shigetoshi Sugawa, and Tadahiro Ohmi**,** *Tohoku University.*

1:35 PM: **Atomistic Simulations of Plasma Process-Induced Si Substrate Damage – Effects of Substrate Bias-Power Frequency –**, Asahiko Matsuda, Yoshinori Nakakubo, Yoshinori Takao, Koji Eriguchi and Kouichi Ono**,** Author, *Kyoto University.*

1:45 PM: **Improvement of gate disturb degradation in SONOS FETs for Vth mismatch compensation in CMOS analog circuits,** Masamichi Suzuki, Atsuhiro Kinoshita and Yuichiro Mitani, *Toshiba Corporation.*

1:55 PM **ESD protection using BIMOS transistor in 100 GHz RF application for advanced CMOS technology,** Philip Galy, *STMicroelectronics.*

Session K – SoC/MPSoC/SIP

Friday, May 31st, 2013

Session Chair: Dac Pham

2:05 PM: *Invited* - **The DOME embedded 64 bit microserver demonstrator,** R. Luijten, *IBM*.

2:20 PM **A fast CAM-based Watermarking extraction on FPGA**, Duc-Hung Le, Tran-Bao-Thuong Cao, Katsumi Inoue and Cong-Kha Pham, *University of Electro-Communications (UEC).*

2:30 PM **I2C System-on-Chip for Bi Dimensional Gas-Sensor Arrays Providing Extended Dynamic-Range A/D Conversion and Row Temperature Regulation,** Fabrizio Conso, Marco Grassi, Claudio De Berti, Piero Malcovati and Andrea Baschirotto, *University of Pavia, Italy.*

2:40 PM: **Bidirectional Interconnect Design for Low Latency High Bandwidth NoC**, Reeshav Kumar, Hrishikesh Deshpande, Gwan Choi, Alex Sprintson and Paul Gratz, *Texas A & M University.*

2:50 PM: Coffee Break

Session L – 3D Integration

Friday, May 31st, 2013

Session Chair: Bich-Yen Nguyen

3:05 PM: **Improving Area and Reliability of Three-Dimensional ICs by Multiplexing Through-Silicon Vias,** Mostafa Said Sayed Abdelrehim, Farhad Mehdipour[1] and Mohamed El-Sayed, *Egypt-Japan University of Science and Technology,[1]Kyushu University.*

3:15 PM: **TSV Count Minimization And Thermal Analysis for 3D Tree-based FPGA,** Vinod Pangracious, Zied Marrakchi[1] and Habib Mehrez, *University Pierre and Marie Curie, [1]FlexRas Technologies Paris.*

3:25 PM: **High-density capacitors for SiP and SoC applications based on three-dimensional integrated,** Wenke Weinreich, Matthias Rudolph, Jan Paul, Johannes Koch, Stefan Riedel, Konrad Seidel, Katja Steidel, Manuela Gutsch, Christoph Hohle and Volkhard Beyer, *Fraunhofer IPMS-CNT.*

3:35 PM: *Invited* - **Stacking™ and Smart Cut™ Technologies for Wafer level 3D Integration,** Mariam Sadaka, Ionut Radu, Chrystelle Lagahe-Blanchard, Lea Di Cioccio, *Soitec USA.*

3:50 PM: *Invited* - **The HfO_2-based RRAM for hybrid Non-volatile Logic circuits,** B. Traore , T.Diokh, K-H Xue, T.Cabout, E.Vianello, G.Molas, L.Perniola, Ph.Blaise, J.F.Nodin, E.Jalaguier and B.de Salvo, *CEA-LETI.*

4:05 PM: Best student paper award

4:15 PM: Closing Remarks

4:25 PM: Presentations of ICICDT 2014

4:35 PM-5:35 PM: Workshop Sessions J, K & L

5:45 PM: Post Conference Meeting for TPC