International Conference on IC Design and Technology (ICICDT)

June 1st – 3rd, 2015
Leuven, Belgium
www.icicdt.org

CONFERENCE PROGRAM

Conference Chair:	Dina H. Triyoso
General Chair:	Keith A. Bowman
Executive Chair:	Thuy B. Dao
Keynote Chair:	Aaron Thean
Local Arrangement Chair:	Wei Guo
Tutorial Chair:	Koji Eriguchi
Publicity & Award Chair:	Mariam Sadaka
Publication Chair:	Ben Kaczer
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This meeting is sponsored by:

UCLouvain EDS Chapter

Tutorial Program

Monday, June 1st, 2015

9:30AM – 10:30AM: Tutorial 1

Demands from security and cryptography on circuits, (devices and process)

Prof. Ingrid Verbauwhede, KU Leuven

Implementing cryptographic algorithms into embedded devices, is a challenge for efficiency reasons as well as security reasons. Because the algorithms use unusual arithmetic, are computationally demanding and often use very large word lengths, it is difficult to fit them into the area, throughput, power and/or energy constraints of the application. Moreover, the implementations have to be made resistant to a wide range of physical attacks, both invasive and non-invasive. We don't want integrated circuits to leak their secrets. Thus adding countermeasures to implementations, adds an extra optimization goal. In this tutorial, the security demands from security and cryptography on circuits (and to lesser degree on process and devices) will be explained. Physically Unclonable Functions and Random Number generators are two essential building blocks in secure implementation. Their design could benefit from a close collaboration between process, device and circuit engineers.

Ingrid Verbauwhede is a Professor in the research group COSIC of the EE Department of the KU Leuven in Belgium. At COSIC, she leads the embedded systems and hardware group. She is also adjunct professor at the EE department at UCLA, Los Angeles, CA. She is a fellow of IEEE, a Member of IACR and she was elected as member of the Royal Academy of Belgium for Science and the Arts in 2011. She received her PhD degree from KU Leuven in 1991 and was a post-doctoral researcher and visiting lecturer at UC Berkeley from 1992 to 1998. She worked for TCSI and the Atmel Design Center in Berkeley, CA from 1994 to 1998. In 1998 she joined UCLA as a tenured associate professor. In 2003 she joined KU Leuven as a professor. Her main interest is in the design and the design methods for secure embedded circuits and systems. She has been general chair and program chair of the IACR CHES conference (Cryptographic Hardware and Embedded Systems), the flagship conference in the field of secure hardware design. She is author or co-author of over 250 publications and 12 patents. Her list of publications and patents is available at www.esat.kuleuven.be/cosic

10:30AM – 11:00AM: Coffee Break

11:00AM – 12:00PM: Tutorial 2

Large-area active matrix sensors for cyber–physical systems

Prof. Tsuyoshi Sekitani, Osaka University

In this talk, I will discuss the recent progresses and future prospects of large-area, ultraflexible, and ultrathin electronic sensors. Our works focus on integration technologies of organic electronics comprising organic thin-film transistors (TFTs), light emitting diodes (LEDs), and photodetectors (PDs) manufactured on thin-film flexible polymeric plastic substrates, which are imperceptible active matrix sensors. Here I would like to demonstrate the applications of imperceptible sensors for sophisticated wearable electronics and real-time health monitoring of civil infrastructures. These sensors serve as an important part of seamless cyberspace/real-world interfaces that are commonly referred to as cyber-physical systems (CPSs). A CPS consists of collaborating computational elements in cyberspace and physical entities in real space, and involves physical sensing (data collection), data transmission and processing, and actuation between cyber and real spaces. The CPS aims to make every social system efficient and optimized. First-generation CPSs can be used in areas as diverse as home security, automotive systems, civil infrastructure, energy, agriculture, healthcare, manufacturing, transportation, robotics, and consumer electronics. Imperceptible electronic sensors are expected to play an increasingly important role in the development of large-area two-dimensional interfaces for collecting physical data in a CPS. On the basis of our initial work on manufacturing different flexible organic devices, including TFTs, LEDs, and PDs, we developed organic flexible electronics for applications that use large-area sensors, actuators, memories, and displays [1-13]. For example, by taking advantage of an ultra flexible and compliant amplifier that can amplify biological signals by 500, we developed 1-μm-thick multi-channel active matrix electrocardiogram and electromyogram monitoring systems. Ultrathin electronics with a total thickness of approximately 1 to 2 μm support a bending radius of less than 10 μm. In addition to the above-mentioned biomedical application, I will also review a wide range of new applications, including real-time health monitoring of civil infrastructures using all-printed large-area sensor systems.

[1] T. Sekitani, et al., Nature Materials, 6, 413 (2007). [2] T. Sekitani, et al., PNAS 105, 4976 (2008). [3] T. Sekitani et al., Science 321, 1468 (2008). [4] T. Sekitani, et al., Nature Materials 8, 494 (2009). [5] T. Sekitani, et al., Science 326, 1516 (2009). [6] T.Sekitani, et al., Nature Materials 9, 1015 (2010). [7] K. Kuribara, et al., Nature Communications 3, 723 (2012). [8] M. Kaltenbrunner, et al., Nature Communications 3, 770 (2012). [9] T. Yokota, et al., IEEE Trans. Electron Devices 59, 3434 (2013). [10] M. Kaltenbrunner, et al., Nature 499, 458 (2013). [11] M. S. White, et. al., Nature Photonics 7, 811 (2013). [12] S. Lee, et. al., Nature Communications 5, 5898 (2014). [13] M. Melzer, et. al., Nature Communications 6, 6080 (2015).

Tsuyoshi Sekitani received the B.S. degree from Osaka University, Japan in 1999, and the Ph.D. degree in applied physics from the University of Tokyo, Japan in 2003. From 1999 to 2003, he was with the Institute for Solid State Physics, the University of Tokyo. From 2003 to 2010, he was a Research Associate, and in 2011, he was an Associate Professor in the School of Engineering at the University of Tokyo. In 2014, he was made a Professor in The Institute of Scientific and Industrial Research at Osaka University. His current research interests include organic transistors, flexible electronics, plastic integrated circuits, large-area sensors, and plastic actuators. He is a member of the Japanese Society of Applied Physics (JSAP) and the Materials Research Society (MRS). He received more than 20 awards including the Paul Rappaport Award in 2009 and 2010 (the Best paper of the IEEE Trans. Electron Devices in 2009 and 2010). In 2014, he was awarded as "Highly Cited Researchers" from THOMSON REUTERS.

12:00PM – 1:30PM: Lunch

1:30PM – 2:30PM: Tutorial 3

Characterization of thermal properties of nanoscale materials/devices and impact of self-heating effects on the performance of advanced transistors

Prof. Ken Uchida, Keio University

The self-heating effect (SHE) is one of the most serious issues in aggressively scaled in field-effect transistors (FETs). In particular, FETs utilizing nanoscale semiconductor as channel materials (nanowire FETs and FinFETs) will severely suffer from SHE. Therefore, the characterization of channel temperature in FETs and device-level thermal management to reduce channel temperature have attracted growing interests. In this work, the techniques to characterize thermal properties of materials as well as transistors will be introduced. Then, the thermal properties of nano materials and nano transistors will be discussed. Finally, strategy to improve the performance of nanoscale FETs by managing the thermal characteristics of devices/interconnects will be given.

Ken Uchida was born in Cambridge, MA in 1971. He received B.S. degree in physics, M.S. and Ph.D. degrees in applied physics all from the University of Tokyo, Tokyo, Japan, in 1993, 1995, and 2002, respectively. In 1995, he joined the Research and Development Center, Toshiba Corporation, Kawasaki, Japan. He has studied carrier transport in nanoscale devices such as Single-Electron Devices, Schottky source/drain MOSFETs, Ultrathin-body SOI MOSFETs, Strained Silicon MOSFETs, Carbon Nanotube Transistors, and (110) Si MOSFETs. In 2008, he moved to Tokyo Institute of Technology, Tokyo, Japan, as an associate professor, where he worked on properties of shallow impurities in nanostructures and modeling of deformation potential in nanoscaled silicon. In 2012, he moved to Keio University, Yokohama, Japan, as a full professor.

2:30PM – 3:00PM: Coffee Break

3:00PM – 4:00PM: Tutorial 4

BTI characterization techniques and application to advanced CMOS devices: finFET, SiGe, Ge and InGaAs

Dr. Jacopo Franco, imec

Reliability and variability are becoming showstoppers for further scaled CMOS technology nodes. The traditional 10 year reliable operation cannot be guaranteed anymore at the single device level, mainly due to severe Bias Temperature Instability (BTI) in high-k gate stacks inducing both degradation of the average device electrical properties, and additional device-to-device variability. Meanwhile, the combination of finFET architectures with high-mobility channel materials is emerging as the frontrunner option to maintain the usual pace of performance enhancement in future technology nodes, opening new questions about device and material reliability. We will first provide a review of BTI characterization. A brief overview of BTI basics will be given, followed by a discussion of more advanced measurement techniques. Analysis of measurements, understanding of results in terms of permanent and recoverable components, and lifetime projections will be covered. Special attention will be given to BTI measurements in nanoscale devices, where the stochastic properties of individual oxide defects become apparent and unveil the relation between BTI degradation and Random Telegraph Noise (RTN). Our recently proposed 'Defect- Centric' model will be shown to capture the time-dependent variability induced by BTI in deeply scaled devices, and to be able to predict end-of-life variability margins to be incorporated in the design of VLSI logic circuits. We will then present a review of our recent studies of BTI in different material systems, highlighting the reliability opportunities and challenges of each novel device family. We will discuss the intrinsic reliability improvement offered by SiGe and Ge pMOS technologies, if a Si cap is used to passivate the channel and to fabricate a standard SiO2/HfO2 gate stack. We will focus on (Si)Ge gate stack optimizations for maximum BTI reliability in planar and finFET device architectures, and on a simple physics-based model able to reproduce the experimental trends. This model framework will be then used to understand the poor BTI reliability and excessive time-dependent variability induced by oxide charge trapping in different high-mobility channel gate stacks as Ge/GeOx/high-k and InGaAs/high-k, independently of the considered device architecture (i.e., planar or finFET). Finally we will discuss how to pursue a reduction of charge trapping in alternative material systems in order to boost the device BTI reliability and minimize time-dependent variability.

Jacopo Franco is a Senior Researcher at imec, Leuven – Belgium. He received the B.Sc.(2005) and M.Sc. (2008) in Electronic Engineering cum laude from the University of Calabria, Italy, and the Ph.D. in Engineering summa cum laude with the Congratulations of the Board of Examiners from KU Leuven, Belgium (2013), defending a Dissertation entitled "Reliability of High Mobility (Si)Ge Channel pMOSFETs for Future CMOS Application—Toward Reliable Ultra-Thin EOT Nanoscale Transistors".

As of Feb. 2013, he holds a permanent position as Senior Researcher in the Device Reliability and Advanced Electrical Characterization (DRE) group of imec. His research interests focus on the reliability of SiGe, Ge and III-V channel transistors for future CMOS nodes and on time-dependent variability issues in nanoscale logic devices. He has (co-)authored more than 120 publications in international journals and conference proceedings, including 20 invited papers, 5 invited presentations, 1 book, 3 book chapters, 10 IEEE International Electron Device Meeting (IEDM) papers, 10 VLSI Technology Symposium papers, 19 IEEE International Reliability Physics Symposium (IRPS) papers, 1 international patent. He is serving or has served at various functions at the IRPS and IIRW (IEEE International Integrated Reliability Workshop) conferences. In 2009 he received the IEEE Nicollian Award for the Best Student Presentation at the IEEE Semiconductor Interface Specialists Conference (SISC). Later on, he received the IEEE Electron Device Society (EDS) Ph.D. Student Fellowship 2012 “for the demonstration of significant ability to perform individual research and a proven record of academic excellence”. He is also one of the recipients of the IEEE Paul Rappaport Award 2011 “for the best paper of the year in the journals of the Electron Device Society”, and of the Best Paper (2012) and Outstanding Paper (2014) awards at IRPS.

Conference Program Overview

Tuesday, June 2nd, 2015

Opening remarks (Dina H. Triyoso) ..... 8:15 AM – 8:30 AM
Keynote Luc Van den hove, imec ..... 8:30 AM – 9:15 AM
Session A: Low Power Memory Technology and Circuits
(Chair: Hideto Hidaka) ..... 9:15 AM – 10:15 AM
Coffee Break ..... 10:15 AM – 10:45 AM
Session B: Emerging Technology
(Chairs: Thomas Ernst and Denis Flandre) ..... 10:45 AM –11:25 AM
Session C: High frequency building blocks
(Chairs: Stefano D'Amico and Andrea Scarpa) ..... 11:25 AM – 11:45 AM
Workshop A, B & C ..... 11:45 AM – 12:45 PM
Lunch ..... 12:45 PM – 1:50 PM
Session D: Advanced Transistors and Materials
(Chairs: Bich-Yen Nguyen and Dina Triyoso) ..... 1:50 PM – 2:50 PM
Session E: Advanced CMOS Device Reliability
(Chairs: Koji Eriguchi and Yuichiro Mitani) ..... 2:50 PM – 3:40 PM
Coffee Break ..... 3:40 PM – 4:10 PM
Session F: CAD and Reliability Challenges in Advanced Technologies
(Chairs: Wei Guo and Thuy Dao) ..... 4:10 PM – 5:00 PM
Workshop D, E &F ..... 5:00PM – 6:00 PM
Reception at Museum ..... 6:30 PM – 8:00 PM

Conference Program Overview

Wednesday, June 3rd, 2015

Opening remarks ..... 8:30 AM – 8:45 AM
Keynote Esin Terzioglu, Qualcomm ..... 8:45 AM – 9:30 AM

Session G: Power Device Reliability and Plasma-Induced Damage
(Chairs: Yuichiro Mitani and Koji Eriguchi) ..... 9:30 AM – 10:10AM
Coffee Break ..... 10:10AM – 10:40 AM
Session H: Analog and Mixed-Signal Techniques
(Chairs: Stefano D'Amico and Andrea Scarpa) ..... 10:40 AM – 11:20 AM
Workshop G & H ..... 11:20 PM – 12:20 PM
Lunch ..... 12:20 PM – 1:30 PM
Session I: High-Power / High-Voltage
(Chairs: Jan Ackaert and Thuy Dao) ..... 1:30 PM – 2:10 PM
Session J: I/O Circuits and ESD Protection
(Chairs: Philippe Galy and Lorenzo Cerati) ..... 2:10 PM – 3:00 PM
Coffee Break ..... 3:00 PM – 3:30 PM
Session K: 3D Integration and Lower Power Processors
(Chairs: Bich-Yen Nguyen and Juergen Pille) ..... 3:30 PM – 4:30 PM
Workshop I, J & K ..... 4:30 PM – 5:30 PM
Awards, Closing Remarks and presentation ICICDT 2016 ..... 5:30 PM – 6:00 PM
Post Conference Meeting (only for TPC) ..... 6:00 PM – 8:00 PM

Conference Program

Tuesday, June 2nd, 2015

8:15 AM Welcome and opening remarks – Dina H. Triyoso

8:30 AM *Keynote*- **From connecting lives to improving lives; the internet of EVERYthing,** Luc Van den hove, President & CEO *imec, Belgium*

Keynote: From connecting lives to improving lives; the internet of EVERYthing

Luc Van den hove, President & CEO *imec*

Several global trends will power further significant growth for semiconductor players. Having reached the point that all persons are connected, the next challenge is to use technology to go beyond connecting people's lives and to effectively improve their lives. Technology will soon provide solutions that will make the world a better, more sustainable place. In healthcare, innovative tools are needed which will transform the way we conduct life science research, diagnose illnesses and treat patients. Tools that will lead to a sustainable healthcare system for everyone, everywhere. The internet of things is rapidly emerging with miniaturized sensors being integrated everywhere. It's hard to imagine a market where sensors, connectivity and mobility will not bring any added value. Besides further evolution in sensor, communication and integration technology, solutions that will allow us to cope with the exponential growth in data are needed. All these innovations have one thing in common: semiconductors as core technology.

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Session A: Low Power Memory Technology and Circuits

Tuesday, June 2nd, 2015

Session Chair: Hideto Hidaka

9:15 AM *Invited* - **Selectors for High Density Crosspoint Memory Arrays: Design Considerations, Device Implementations and Some Challenges Ahead,** Govoreanu, Bogdan; Zhang, Leqi; Jurczak, Malgorzata, *imec, Leuven, Belgium*

9:25 AM **Current Pulse Generator for Multilevel Cell Programming of Innovative PCM**, Kiouseloglou, Athanasios (1,2); Navarro, Gabriele (1); Cabrini, Alessandro (2); Torelli, Guido (2); Perniola, Luca (1), *1: CEA-LETI, MINATEC Campus, France; 2: University of Pavia, Italy.*

9:35 AM **Design Technology Co-optimization for Enabling 5nm gate-all-around Nanowire 6T SRAM**, Huynh-Bao, Trong (1,2); Sakhare, Sushil (1); Ryckaert, Julien (1); Yakimets, Dmitry (1,3); Mercha, Abdelkarim (1); Verkest, Diederik (1,2); Thean, Aaron Voon-Yew (1); Wambacq, Piet (1,2), *1: imec, Belgium; 2: ETRO, Vrije Universiteit Brussel; 3: ESAT, Katholieke Universiteit Leuven.*

9 45 AM **Assessment of SiGe Quantum Well transistors for DRAM peripheral applications**, Ritzenthaler, Romain (1); Schram, Tom (1); Spessot, Alessio (2); Eneman, Geert (1); Noh, Kyung-Bong (3); Son, Yunik (3); Aoulaiche, Marc (2); Fazan, Pierre (2); Mocuta, Anda (1); Horiguchi, Naoto (1); Thean, Aaron (1) *1: imec, Belgium; 2: micron Belgium, Belgium; 3: SK-Hynix.*

9:55 AM **Low Standby Power Capacitively Coupled Sense Amplifier for Wide Voltage Range Operation of Dual Rail SRAMs,** Grover, Anuj (1); Visweswaran, G. S. (2); Parthasarathy, Chittoor (3); Daud, Mohammad (1); Moritz, Guillaume (4); Noel, Jean-Philippe (3); Giraud, Bastien (4); Turgis, David (3); Kumar, Promod (1) *1: STMicroelectronics Ltd., India; 2: Indian Institute of Technology Delhi, India; 3: STMicroelectronics Ltd., France; 4: CEA LETI, France.*

10:05 AM **A 6T-SRAM in 28nm FDSOI Technology with Vmin of 0.52V Using Assisted Read and Write Operation,** Kumar, Ashish (1); Visweswaran, G.S. (2); Saha, Kaushik (2); Kumar, Vinay (1); Janardan, Dhori Kedar (1), *1: STMicroelectronics Pvt. Ltd., India; 2: Indian Institute of technology, New Delhi, India.*

10:15 AM Coffee Break

Session B – Emerging Technologies

Tuesday, June 2nd, 2015

Session Chairs: Thomas Ernst and Denis Flandre

10:45 AM *Invited* - **NEMS switches: challenges and opportunities in emerging IC technologies,** Feng, Philip X.-L., *Case Western Reserve University, Cleveland, USA.*

10:55 AM **Wide Band Study of Silicon-on-Insulator Photodiodes on Suspended Micro-Hotplates Platforms**, André, Nicolas (1); Li, Guoli (1,2); Gérard, Pierre (1); Poncelet, Olivier (1); Zeng, Yun (2); Ali, Zeeshan (3); Udrea, Florin (3,4); Francis, Laurent (1); Flandre, Denis (1), *1: UC Louvain, Belgium; 2: Hunan University, China; 3: Cambridge CMOS Sensors, UK; 4: University of Cambridge, UK.*

11:05 AM **Evaluation of 32-Bit Carry-Look-Ahead Adder Circuit with Hybrid Tunneling FET and FinFET Devices,** Wu, Tse-Ching; Chen, Chien-Ju; Chen, Yin-Nien; Hu, Vita Pi-Ho; Su, Pin; Chuang, Ching-Te, *National Chiao Tung University, Taiwan, Republic of China.*

11:15 AM **Area and Routing Efficiency of SWD Circuits Compared to Advanced CMOS**, Zografos, Odysseas (1,2); Raghavan, Praveen (1); Sherazi, Yasser (1,2); Vaysset, Adrien (1,2); Ciubatoru, Florin (1,2); Sorée, Bart (1,2); Lauwereins, Rudy (1,2); Radu, Iuliana (1); Thean, Aaron (1), *1: imec, Belgium; 2: ESAT - KU Leuven, Belgium.*

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Session C – High frequency building blocks

Tuesday, June 2nd, 2015

Session Chairs: Stefano D'Amico and Andrea Scarpa

11:25 AM **A 180-nm CMOS RF Transmitter for UHF RFID Reader,** Nguyen, Khanh, *Integrated Circuit Design Research and Education Center (ICDREC), Vietnam National University, Vietnam.*

11:35 AM **Low-Phase Noise Variation VCO Implementing Resistorless Digitally Controlled Varactor**, Aqeeli, Mohammed Ali, *University of Manchester, United Kingdom.*

11:45 AM – 12:45PM Workshop Sessions A, B & C

12:45 PM – 1:50PM Lunch

Session D: Advanced Transistors and Materials

Tuesday, June 2nd, 2015

Session Chairs: Bich-Yen Nguyen and Dina H. Triyoso

1:50 PM *Invited* - **Dimensioning for power and performance under 10nm: the limits of FinFETs scaling**, Garcia Bardon, M; Schuddinck, P.; Raghavan, P.; Jang, D.; Yakimets, D.; Mercha, A.; Verkest, D.; Thean, A., *imec, Leuven, Belgium*

2:00 PM **Impact of Fin Shape Variability on Device Performance towards 10nm Node**, Tomida, Kazuyuki (1); Hiraga, Keizo (1); Dehan, Morin (2); Hellings, Geert (2); Jang, Doyoung (2); Miyaguchi, Kenichi (2); Chiarella, Thomas (2); Kim, Minsoo (2); Mocuta, Anda (2); Horiguchi, Naoto (2); Mercha, Abdelkarim (2); Verkest, Diederik (2); Thean, Aaron (2). *1: Sony, Japan; 2: imec, Belgium.*

2:10 PM **Modeling FinFET Metal Gate Stack Resistance for 14nm Node and Beyond**, Miyaguchi, Kenichi; Parvais, Bertrand; Ragnarsson, Lars-Åke; Wambacq, Piet; Raghavan, Praveen; Mercha, Abdelkarim; Mocuta, Anda; Verkest, Diederik; Thean, Aaron, *imec, Belgium.*

2:20 PM *Invited* - **Static and Dynamic Power management in 14nm FDSOI technology,** Weber, O; Josse, E.; Mazurier, J.; Haond, M, *LETI, France.*

2:30 PM **Lateral NWFET Optimization for Beyond 7nm Nodes**, Yakimets, Dmitry (1,2); Jang, Doyoung (2); Raghavan, Praveen (2); Eneman, Geert (2); Mertens, Hans (2); Schuddinck, Pieter (2); Mallik, Arindam (2); Garcia Bardon, Marie (2); Collaert, Nadine (2); Mercha, Abdelkarim (2); Verkest, Diederik (2); Thean, Aaron (2); De Meyer, Kristin (1,2), *1: KU Leuven, Belgium; 2: imec,Leuven, Belgium.*

2:40 PM **Nonparabolicity and confinement effects of III-V materials in novel transistor**, Pourghaderi, M. Ali; Mocuta, Anda; Thean, Aron, *imec, Belgium.*

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Session E – Advanced CMOS Device Reliability

Tuesday, June 2nd, 2015

Session Chairs: Koji Eriguchi and Yuichiro Mitani

2:50 PM *Invited* - **PBTI for n-type Tunnel FinFETs,** Mizubayashi, W.; Mori, T.; Fukuda, K.; Liu, Y. X.; Matsukawa, T.; Ishikawa, Y.; Endo, K.; O'uchi, S.; Tsukada, J.; Yamauchi, H.; Morita, Y.; Migita, S.; Ota, H.; Masahara, M., *National Institute of Advanced Industrial Science and Technology (AIST), Japan.*

3:00 PM **Reliability impact of Advanced Doping techniques for DRAM peripheral MOSFETs,** Spessot, Alessio (1); Ritzenthaler, Romain (2); Schram, Tom (2); Aoulaiche, Marc (1); Cho, Moonju (2); Luque, Maria Toledano (2); Horiguchi, Naoto (2); Fazan, Pierre (1), *1: Micron Technology Belgium, imec Campus, Belgium; 2: imec, Belgium.*

3:10 PM **Impact of Random Telegraph Noise on Ring Oscillators Evaluated by Circuit-level Simulations,** Oshima, Azusa (1); Weckx, Pieter (2); Kaczer, Ben (2); Kobayashi, Kazutoshi (1); Matsumoto, Takashi (3), *1: Kyoto Institute of Technology, Japan; 2: imec, Belgium; 3: Kyoto University, Japan.*

3:20 PM **Simple Technique for Prediction of Breakdown Voltage of Ultrathin Gate Insulator under ESD Testing,** Mitani, Yuichiro; Matsuzawa, Kazuya, *Toshiba Corporation, Japan.*

3:30 PM **Off-State Stress degradation mechanism on advanced p-MOSFETs,** Cho, Moonju (1); Spessot, Alessio (2); Kaczer, Ben (1); Aoulaiche, Marc (2); Romain, Ritzenthaler (1); Tom, Schram (1); Pierre, Fazan (2); Naoto, Horiguchi (1); Linten, Dimitri (1), *1: imec, Belgium; 2: Micron Technology Belgium.*

3:40 PM Coffee Break

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Session F - CAD and Reliability Challenges in Advanced Technologies

Tuesday, June 2nd, 2015

Session Chair: Wei Guo and Thuy Dao

4:10 PM *Invited* - **Deadspace-aware Power/Ground TSV Planning in 3D Floorplanning,** Wang, Shengcheng; Firouzi, Farshed; Oboril, Fabian; Tahoori, Mehdi, *Karlsruhe Institute of Technology, Germany.*

4:20 PM **Impact of Device and Interconnect Process Variability on Clock Distribution**, Fiévet, Nathalie (1); Raghavan, Praveen (2); Baert, Rogier (2); Robert, Frédéric (1); Mercha, Abdelkarim (2); Verkest, Diederik (2); Thean, Aaron (2), *1: Université Libre de Bruxelles, Belgium; 2: imec, Belgium.*

4:30 PM *Invited* - **Impact of time-dependent variability on the yield and performance of 6T SRAM cells in an advanced HK/MG technology,** Weckx, Pieter (1,2); Kaczer, Ben (1); Roussel, Philippe J. (1); Catthoor, Francky (1,2); Groeseneken, Guido (1,2), *1: imec, Belgium; 2: KU Leuven.*

4:40 PM **Countering Early Propagation and Routing Imbalance of DPL Designs in a Tree-based FPGA,** Amouri, Emna; Bhasin, Shivam; Mathieu, Yves; Graba, Tarik; Danger, Jean-Luc, *Telecom Paris Tech, France.*

4:50 PM **FinFET Stressor Efficiency on Alternative Wafer and Channel Orientations for the 14 nm Node and Below**, Eneman, Geert; De Keersgieter, An; Mocuta, Anda; Collaert, Nadine; Thean, Aaron, *imec, Belgium.*

5:00 PM – 6:00 PM Workshop Sessions D, E & F

6:30 PM – 8:00 PM Reception at Museum M

Conference Program

Wednesday, June 3rd, 2015

8:30 AM Opening remarks

8:45 AM *Keynote*-**Design And Technology Co-Optimization For Mobile SOCs**, Esin Terzioglu, *Qualcomm, USA.*

Keynote: Design And Technology Co-Optimization For Mobile SOCs

Esin Terzioglu, Vice President Engineering, Qualcomm

Mobile System-on-Chip design and technology requirements are driven by typical 1-year product cycle of premium tier devices. There are expectations of improved performance, power and cost metrics delivered by design-technology teams on a yearly cadence. In order to respond to market requirements, we have been following an annual technology cadence to deliver improved product specifications. As traditional Moore's Law slows, keeping pace requires additional design and design-technology co-optimization efforts to claim full benefits of a new advanced silicon technology node to meet market needs.

This talk gives an overview of the challenges of design-technology interactions and optimizations targeted for mobile applications where the products are constrained in size, battery capacity, peak power, thermal envelope and require increasing overall performance. Advanced technology node challenges such as multiple patterning, increased variability and device parasitics limitations have to be addressed through a combination of technology-IP co-definition, optimized library design targeted for each application, customized statistical design methodologies and tools to claim full scaling benefit of power, performance and area/cost. Additional challenges emerge due to increased power density reaching thermal limits of product form factor as well as silicon SoC itself. Packaging has to be compact to fit into increasingly thin product designs, dissipate heat generated on the SoC and deliver power with minimal losses.

Moore's Law continues to deliver benefits of scaling and will continue to do so into the foreseeable future. Challenges require tight collaboration between research institutions, foundries, EDA and design-technology teams in a new industry-wide working model.

Session G – Power Device Reliability and Plasma-Induced Damage

Wednesday, June 3rd, 2015

Session Chairs: Yuichiro Mitani and Koji Eriguchi

9:30 AM *Invited* - **Trapping induced parasitic effects in GaN-HEMT forpower switching applications,** Meneghesso, Gaudenzio (1); Meneghini, Matteo (1); Zanoni, Enrico (1); Vanmeerbeek, Piet (2); Moens, Peter (2), 1: *University of Padova, Italy, 2: ON Semiconductors, Oudenaarde, Belgium.*

9:40 AM **Plasma Induced Damage Investigation in the Fully Depleted SOI Technology,** Akbal, Madjid (1); Ribes, Guillaume (1); Vallier, Laurent (2) *1: STMicroelectronics, France; 2: LTM/CNRS, France.*

9:50 AM **Plasma-induced photon irradiation damage on low-k dielectrics enhanced by Cu-line layout,** Ikeda, Taro (1); Eriguchi, Koji (2); Tanihara, Akira (1); Yamamoto, Nobuhiko (1); Kasai, Shigeru (1); Ono, Kouichi (2) *1: Tokyo Electron Yamanashi Limited, Japan; 2: Kyoto University, Japan.*

10:00 AM **Surface Orientation Dependence of Ion Bombardment Damage during Plasma Processing,** Okada, Yukimasa; Eriguchi, Koji; Ono, Kouichi, *Kyoto University, Japan.*

10:10 AM Coffee Break

International Conference on IC Design and Technology (ICICDT)

June 1st – 3rd, 2015
Leuven, Belgium
www.icicdt.org

Session H - Analog and Mixed-Signal Techniques

Wednesday, June 3rd, 2015

Session Chair: Stefano D'Amico and Andrea Scarpa

10:40 AM *Invited* - **High-Speed Analog-to-Digital Converters in downscaled CMOS,** Spagnolo, Annachiara (1); Verbruggen, Bob (2); D'Amico, Stefano (3); Wambacq, Piet (1,4), *1: imec, Leuven, Belgium; 2: Xilinx, Dublin, Ireland, 3: Universitá del Salento - Lecce, Italy, 4:Vrije Universiteit Brussel - Brussels, Belgium*

10:50 AM **Methods to increase linearity of high-performance ADC**, Fan, Hua (1); Liu, Kehong (1); Liu, Airong (2); Lv, Lishan (1); Qiao, Zhiliang (1); Li, Qiang (1), *1: University of Electronic Science and Technology of China, Chengdu, China; 2: Institute of Semiconductors, Chinese Academy of Sciences, Beijing, China.*

11:00AM **Optimal Design to Maximize Efficiency of Single-Inductor Multiple-Output Buck Converters in Discontinuous Conduction Mode for IoT Applications,** Yamauchi, Yoshitaka; Yanagihara, Yuki; Fuketa, Hiroshi; Sakurai, Takayasu; Takamiya, Makoto, *University of Tokyo, Japan.*

11:10 AM **A Self-Reference Sense Amplifier in Low Power EEPROM,** Tay, Ho Quang (1); Tu, Bui Trong (2); Linh, Mai (3), *1: ICDREC, VNU-HCM, Vietnam; 2: University of Science, VNU-HCM, Vietnam; 3: International University, VNU-HCM, Vietnam.*

11:20 AM – 12:20 PM Workshop Sessions G, & H

12:20 PM – 1:30PM Lunch

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Session I - High-Power / High-Voltage

Wednesday, June 3rd, 2015

Session Chairs: Jan Ackaert and Thuy Dao

1:30 PM *Invited* - **Thermal experimental and modeling analysis of high power 3D packages,** Oprins, Herman (1); Cherman, Valdimir (1); Van der Plas, Geert (1); Maggioni, Federica (1,2); De Vos, Joeri (1); Beyne, Eric (1), *1: imec, Belgium; 2: Dept. Mechanical Engineering, K.U. Leuven, Belgium.*

1:40 PM **Metallization scheme optimization of plastic-encapsulated electronic power devices,** Ackaert, Jan (1); Malik, Aditi (2); Gonzalez, Mario (3) *1: ON semiconductors, Belgium; 2: ON semiconductors, USA; 3: imec, Belgium.*

1:50 PM **I/O thick oxide device integration using Diffusion and Gate Replacement (D&GR) gate stack integration,** Ritzenthaler, Romain (1); Schram, Tom (1); Spessot, Alessio (2); Caillat, Christian (2); Aoulaiche, Marc (2); Cho, Moonju (1); Noh, KyungBong (3); Son, Yunik (3); Fazan, Pierre (2); Mocuta, Anda (1); Horiguchi, Naoto (1); Thean, Aaron (1), *1: imec, Belgium; 2: Micron Belgium, Belgium; 3: SK-Hynix.*

2:00 PM **Characterization of Onset Tunneling Voltage (Vonset) Walkout in High-Voltage Deep Trench Isolation on SOI,** Dao, Thuy (1); Ger, Mu-Ling (2); Zuo, Jiangkai (1), *1: Freescale, Austin, USA; 2: Freescale, Tempe, USA.*

Session J – I/O Circuits and ESD Protection

Wednesday, June 3rd, 2015

Session Chairs: Philippe Galy and Lorenzo Cerati

2:10 PM *Invited* - **Integrated Front-End/Back-End Simulation of Electromagnetic Fields, Lorentz Force Effects and Fast Current Surges in Microelectronic Protection Devices,** Schoenmaker, Wim (1); Galy, Philippe (2), *1:* Magwel; *2: STMicroelectronics, France.*

2:20 PM **Impact of local interconnects on ESD design**, Scholz, Mirko (1); Chen, Shih-Hung (1); Hellings, Geert (1); Boschke, Roman (2); Linten, Dimitri (1), *1: imec, Belgium; 2: imec, Belgium and K.U. Leuven, Belgium.*

2:30 PM **ESD protection diodes in Optical interposer technology**, Boschke, Roman (1,2); Groeseneken, Guido (1,2); Scholz, Mirko (1); Chen, Shih-Hung (1); Hellings, Geert (1); Verheyen, Peter (1); Linten, Dimitri (1), *1: imec, Leuven, Belgium; 2: K.U. Leuven, Belgium.*

2:40 PM **Preliminary 3D TCAD Electro-thermal Simulations of BIMOS transistor in thin silicon film for ESD protection in FDSOI UTBB CMOS technology,** Athanasiou, Sotirios (1,2); Cristoloveanu, Sorin (2); Galy, Philippe (1), *1: STMicroelectronics, France; 2: IMEP, France.*

2:50 PM **A High-Speed 2xVDD Output Buffer With PVTL Detection Using 40-nm CMOS Technology**, Wang, Chua-Chin; Tsai, Tsung-Yi; Lin, Wei, *National Sun Yat-Sen University, Taiwan, Republic of China*.

3:00 PM Coffee Break

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Session K – 3D Integration and Lower Power Processors

Wednesday, June 3rd, 2015

Session Chairs: Bich-Yen Nguyen and Juergen Pille

3:30 PM: *Invited* - **3D Monolithic Integration: stacking technology and applications,** Radu, Ionut; Nguyen, Bich-Yen; Gaudin, Gweltaz; Mazure, Carrlos, *Soitec, USA.*

3:40 PM **Through Silicon Via to FinFET noise coupling in 3-D integrated circuits**, Rouhi Najaf Abadi, Alireza (1,2); Guo, Wei (1); Sun, Xiao (1); Ben Ali, K. (3); Raskin, J.P (3); Rack, M. (3); Roda Neve, Cesar (1); Choi, M. (4); Moroz, V. (4); Van der Plas, Geert (1); De Wolf, Ingrid (1); Beyne, Eric (1); Absil, Philippe (1), *1: imec, Belgium; 2: K.U. Leuven, Belgium; 3: ICTEAM, Université Catholique de Louvain, Belgium; 4: SYNOPSYS, Mountain View, USA.*

3:50 PM **Simple Wafer Stacking 3D-FPGA Architecture,** Amagasaki, Motoki; Zhao, Qian; Iida, Masahiro; Kuga, Morihiro; Sueyoshi, Toshinori, *Kumamoto Univ., Japan.*

4:00 PM *Invited* - **3DIC Challenges and Achievements,** Vardaman, Jan; Bal, Linda, *TechSearch Intl, Inc, USA.*

4:10 PM **Design of a Low-power Fixed-point 16-bit Digital Signal Processor Using 65nm SOTB Process,** Le, Duc-Hung (1); Sugii, Nobuyuki (2); Kamohara, Shiro (2); Nguyen, Xuan-Thuan (1); Ishibashi, Koichiro (1); Pham, Cong-Kha (1), *1: The University of Electro-Communications, Japan; 2: Low-power Electronics Association & Project.*

4:20 PM *Invited* - **Power measurements and cooling of the DOME 28nm 1.8GHz 24-thread ppc64 µServer compute node,** Luijten, Ronald P.; Cossale, Matteo; Clauberg, Rolf; Doering, Andreas, *IBM Research - Zurich, Switzerland.*

4.30 PM – 5.30 PM Workshop Sessions I, J & K

5:30 PM Best student paper award

5:45 PM – 6.00PM Closing Remarks & Presentation of ICICDT 2016

6:00 PM Post Conference Meeting (only for TPC)