**IEEE Joint Conference**

**International Conference on IC Design and Technology (ICICDT)**

**&**

**Solid State Systems Symposium (4S)**

June 27th – 29th, 2016

Ho Chi Minh City, Vietnam

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# CONFERENCE PROGRAM

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| Conference Co-Chair: | Dang Luong Mo |
| General Chair: | Dina H. Triyoso |
| Executive Chair: | Thuy B. Dao |
| Local Arrangement Chair: | Bich-Yen Nguyen |
| Tutorial Chair: | Andrea Scarpa |
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# Tutorial Program

## Monday, June 27th, 2016

### 9:30AM – 10:30AM: Tutorial 1

### "Circuit and Device Interactions for Nonvolatile Memory in IoT Era"

**Prof. Meng-Fan (Marvin) CHANG, National Tsing Hua University (NTHU), Taiwan**

Memory has become one of the bottlenecks in the development of IoT and wearable devices with low energy consumption. This tutorial addresses trends in the development of nonvolatile memory (NVM) for energy-efficient IoT applications. We will examine a variety of NVM technologies, including Flash, resistive RAM (ReRAM), and phase-change memory (PCM). This tutorial will explore the challenges faced by researchers in the device and circuit interactions for nonvolatile memory. We will also look at some state-of-the-art silicon-verified device-circuit integration techniques, including high-speed, low-power and endurance-extension NVM macros. The requirement and implementation of NVM devices beyond conventional applications, such as nonvolatile-logics (nvLogics) for nonvolatile processors, will also be discussed.

**Meng-Fan Chang** is a full Professor in the Dept. of Electrical Engineering of National Tsing Hua University (NTHU), Taiwan. Since 2011, he has also served as the Associate Executive Director of National Program for Intelligent Electronics (NPIE) in Taiwan during 2011-2016. Dr. Change obtained considerable practical experience before joining NTHU in 2006, having spent more than ten years working in industry.
Between 1997 and 2006, Dr. Chang worked in the development of SRAM/ROM/Flash macros/compilers at Mentor Graphics (New Jersey, US), TSMC (Taiwan), and the Intellectual Property Library Company (Taiwan). He has been service as an associate editor for IEEE TVLSI, IEEE TCAD and IEICE Electronics. He has been serving on technical program committees for ISSCC, IEDM, A-SSCC, ISCAS, and numerous international conferences. His research interests include circuit design for volatile and nonvolatile memory, 3D-Memory, spintronics and memristor logics, computing-in-memory, and circuit-device-interactions in non-CMOS devices.

### 10:30AM – 11:00AM: Coffee Break

**11:00AM – 12:00PM: Tutorial 2**

## "Technology trends and applications of embedded STT-MRAM from big data to wearable devices"

**Dr. Shinobu Fujita, Toshiba Corp.,Japan**

Recently, advanced embedded STT-MRAM technologies expected for high-speed and low-power embedded memory applications have been mature. Advancement of embedded STT-MRAM technologies will be overviewed to clarify their advantageous features such as a high-speed access, a novel scalability and normally-off + instant-on mode. Then, various applications from big data to wearable and IoT devices will be presented, and issues regarding their applications will also be addressed. Furthermore, future challenges regarding technologies and application will be analyzed.

**Shinobu Fujita** took PhD of University of Tokyo in 1989. He joined Toshiba in 1989. He has been working for new applications based on nonvolatile memory for over 10 years. Currently, he is a Chief Research Scientist of Toshiba Corporate R&D Center and leading a project for development of embedded STT-MRAM cache systems based on Normally-off Computing.

**12:00PM – 1:30PM: Lunch**

## 1:30PM – 2:30PM: Tutorial 3

# "Reliability Physics of SiO2 and High-k Dielectric Films for CMOS, RF, and Power Devices"

**Dr. Kenji Okada, TowerJazz Panasonic Semiconductor (TPSCo), Japan**

Reliability has been regarded as the showstopper of various kinds of state-of-the-art devices. To achieve further advance of these devices, both reliability and device performance must be well balanced and kept at the extremely high levels. This is valid not only for the extremely scaled CMOS devices, but also for various power and RF/MMIC devices processed on Si, GaN, GaAs, SiC and so on. For this purpose, deeper understandings on the physics of various reliability items such as TDDB, SILC, NBTI, PBTI, and HC are crucial as well as that on the device performance. Therefore, in this tutorial, reliability physics will be discussed with focusing on the dielectric films used as the gate dielectrics, tunnel dielectrics, capacitor films, and so on in each device. Thickness of dielectrics discussed in this tutorial is very wide, from ~1.5 to ~40 nm. This tutorial discusses dielectric films developed for devices in the following opposite directions:

(1) EOT scaling of gate dielectrics in CMOS 'system LSI' devices (~1.5 to ~10 nm), and,
(2) very thick SiO2-base and Si3N4-base dielectric films (~10 to ~40 nm) used in power and RF/MMIC devices and also used as inter-metal dielectrics (IMD).

As for the EOT scaling direction (1), mechanisms and models for various reliability items will be discussed, followed by the discussions on the alteration of models due to the scaling and to the introduction of new materials such as metal gate electrode and high-k gate dielectrics. For example, with the thinning of gate dielectrics, the soft breakdown, which we reported for the first time as the 'B-mode SILC' and 'B-mode shift', becomes observable even by conventional measurements. Appearance of soft breakdown strongly required us to change the lifetime prediction method. Furthermore, the introduction of high-k materials to the gate stack structure required us to take into account the existence of high density initial traps. High density initial traps let us misunderstand the TDDB statistics and also increased the importance of BTI degradation.

As for the very thick dielectric films (2), anomalous TDDB statistics which prevents us from appropriately predicting the lifetime with conventional methods will be discussed with SiO2-base gate dielectrics and Si3N4 films in MIM capacitors. The cause of this anomalous TDDB statistics is just an intrinsic and simple event, that is, the carrier charging into initial and stress-generated traps and, hence, no one can free from this anomalous TDDB statistics regardless of the material. Impact of this charging-induced dynamic stress relaxation (CiDSR) effect on various parameters in TDDB statistics will be demonstrated.

**Kenji Okada** received the B.S. and the M.S. degrees in the materials science from Osaka University, Osaka, Japan, in 1985 and 1987, respectively. He joined the Semiconductor Research Center, Matsushita Electric Industrial Co., Ltd (Panasonic Corporation), Osaka, Japan, in 1987. He had been engaged in the research and developments of the gate and tunnel dielectrics used in Si MOS and flash memory devices, and received the Ph.D. from Osaka University, Osaka, Japan, in 2003. From 2004 to 2007, he was with the Millennium Research for Advanced Information Technology (MIRAI) project, Tsukuba, Japan, and investigated the reliability physics of high-k stacked gate dielectrics such as TDDB, NBTI, and PBTI. From 2008 to 2013, he engaged in the research and development of various advanced devices at Panasonic, such as Si system LSI with high-k/metal gate, CMOS and CCD image sensors, power devices including GaN and SiC from the viewpoint of device reliabilities as a manager of reliability development team. Since 2014, he has been with Process Technology Center, TowerJazz Panasonic Semiconductor Co., Ltd. (TPSCo), where he continues his investigation on the reliability physics of various devices. He served on the technical committees of IEEE Semiconductor Interface Specialists Conference (SISC, 2000~2002), IEEE International Electron Devices Meeting (IEDM, 2001~2002 and 2010~2011), IEEE International Reliability Physics Symposium (IRPS, 2003, 2006, 2007, and 2016), and so on. He also served as an editor of Japanese Journal of Applied Physics (JJAP) from 2000 to 2008. Dr. Okada is a member of the Japan Society of Applied Physics and also of the IEEE Electron Device Society and Reliability Society.

**2:30PM – 3:00PM: Coffee Break**

**3:00PM – 4:00PM: Tutorial 4**

## "Technologies for developing a successful IoT MCU chip"

**Mr. Lei (Jerry) Zhang**

MCU as the terminal of IoT or indispensable component in the server, which request higher capability on connectivity, with lowest power consumption for portable application. This tutorial will give an overview of technologies widely used in MCU chip design and integration. It will illustrate several topics, the approaches to lower down dynamic and static power consumptions via process, architecture and synthesis; the signal integrities of analog and RF IPs; the IO concerning for high performance EMC compliant; and general security protection methods in the chip. A practicable developing flow also been introduced to demonstrate the real engineering works behind a chip.

**Lei Zhang** achieved a Master Degree in NanYang Tech. Univ. and MBA in Xi'an JiaoTong University. He has been a Senior SoC design Manager in NXP (Previous Freescale) Semiconductor Micro- Group since 2011. He is focus on MCU architecture and RTL2GDS chip developing. He leads the team built 11 dice in ARM Based Kinetis family and four new generation 8-Bits products on different technic notes. 50% of them were successfully goes to mass production with only one Tape-Out.
From 1998 to 2011, he worked in Infineon Technologies Automotive and Industry Group, as a technical lead and design manager, focus on 32bit-Tricore and 8/16-Bits MCU develop. He accumulates abundant skill on circuit design, top-level integration, timing closure, verification and DFT. He also worked in China Academic of Science on Analog circuit design for four years from 1994.
He has several publications in EDA and IEEE conference on Signal Integrity for timing and power analysis, as well as chip level Dynamic Frequency & Power Management. He holds patents in digital and analog circuit design area. He also got certificate of Infineon Project Manager Academic Assessment. And he has ever been the Lecturer of Xi'an JiaoTong University in EE Department.

# Conference Program Overview

## Tuesday, June 28th, 2016

**Opening remarks (Dang Luong Mo)** ..... 8:00 AM – 8:30 AM

**Keynote1: Uming Ko, MediaTek** ..... 8:30 AM – 9:15 AM
**Session A: Low-Power Circuits & Technology**
**(Chair: Tran Xuan Tu)** ..... 9:15 AM – 9:55 AM
**Coffee Break** ..... 9:55 AM – 10:10 AM
**Session B: Reliability and Soft Error**
**(Chairs: Koji Eriguchi and Yuichiro Mitani)** ..... 10:10 AM –10:50 AM
**Session C: I/O Circuits and ESD Protection**
**(Chairs: Lorenzo Cerati and Philippe Galy)** ..... 10:50 AM –11:10 AM
**Workshop A, B & C** ..... 11:10 AM – 12:10 PM

**Lunch** ..... 12:10 PM – 1:05 PM

**Keynote2: Yoshikazu Nitta, Sony Corporation** ..... 1:05 PM – 1:50 PM
**Session D: Advanced Transistors/Materials and High Power/High Voltage**
**(Chairs: Bich-Yen Nguyen and Wenke Weinreich)** ..... 1:50 PM – 3:00 PM
**Coffee Break** ..... 3:00 PM – 3:15 PM
**Session E: RF&Analog Mixed Signal**
**(Chair: Cuong Huynh and Dina Triyoso)** ..... 3:15 PM – 4:15 PM
**Workshop D & E** ..... 4:15PM – 5:15 PM

**Dinner Reception at Hotel Majestic Saigon** ..... 6:30 PM – 8:00 PM

# Conference Program Overview

## Wednesday, June 29th, 2016

**Opening remarks (Yuichiro Mitani)** ..... 8:00 AM – 8:15 AM

**Keynote3: Thang Tran, Synopsys** ..... 8:15 AM – 9:00 AM
**Session F: SoC/MPSoC/SIP & CAD/DFX**
**(Chairs: Dac Pham, Juergen Pille, and Rouwaida Kanj)** ..... 9:00 AM – 10:10AM
**Coffee Break** ..... 10:10AM – 10:30 AM
**Session G: Advanced Memory Devices**
**(Chair: Hideto Hidaka)** ..... 10:30 AM – 11:20 AM
**Workshop F & G** ..... 11:20 PM – 12:20 PM

**Lunch** ..... 12:20 PM – 1:20 PM

**Keynote4: Sommawan Khumpuang, AIST** ..... 1:20 PM – 2:05 PM
**Session H: Minimal Fab Application**
**(Chairs: Dang Luong Mo and Sommawan Khumpuang)** ..... 2:05 PM – 2:35 PM
**Coffee Break** ..... 2:35 PM – 2:55 PM
**Session I: 3D Integration & Emerging Technologies**
**(Chairs: Thomas Ernst and Thuy Dao)** ..... 2:55 PM – 3:55 PM
**Workshop H & I** ..... 3:55 PM – 4:55 PM
**Best student paper award** ..... 4:55 PM – 5:10 PM
**Closing Remarks & Presentation of ICICDT 2017** ..... 5:10 PM – 5:25 PM
**Post Conference Meeting for TPC** ..... 6:00 PM – 8:00 PM

# Conference Program

## Tuesday, June 28th, 2016

8:00 AM Welcome and opening remarks – Dang Luong Mo

8:30 AM *Keynote 1*-**Low Power CPU: from Mobile to Wearable & IoT**, Uming Ko, *MediaTek, USA*

## Keynote 1: Low Power CPU: from Mobile to Wearable & IoT

Uming Ko, MediaTek VP of Technology

With the landmark introduction of Smartphone in 2007, Mobile Internet and computing took off and the associated data bandwidth has ever-since grown exponentially resulting in the ever-increasing computing requirements. However, mobile CPU will soon hit the frequency and thermal limits. Thus, mobile clients are rapidly moving to multi-core CPU/GPU with system-adaptive power management, thermal throttling, and heterogeneous multi-processing. The insatiable computation need, coupled with the explosion of Internet-of-Things (IoT) that demands long battery operation, further presents major thermal and energy gaps. Consequently, many innovations are desperately needed to enable the ubiquitous ecosystem that promises to provide ample possibilities to enhance and enrich everyone's life.

# Session A: Low-Power Circuits & Technology

## Tuesday, June 28th, 2016

## Session Chair: Tran Xuan Tu

9:15 AM **A High-Throughput and Low-Power Design for Bitmap Indexing on 65-nm SOTB CMOS Process**, Xuan-Thuan Nguyen, Hong-Thu Nguyen, and Cong-Kha Pham, The University of Electro-Communications, Tokyo, Japan.

9:25 AM **Ultra Low-Power and Low-Energy 32-bit Datapath AES Architecture for IoT Applications**, Duy-Hieu Bui(1); Diego Puschini(1); Simone Bacles-Min(1); Edith Beigné(1); Xuan-Tu Tran(2), *1:Université Grenoble Alpes, Grenoble, FRANCE,2:VNU University of Engineering and Technology, Hanoi, Vietnam.*

9:35 AM **A Compact, Low Power AES Core on 180nm CMOS Process**, Van-Lan Dao; Van-Phuc Hoang; Anh-Thai Nguyen; Quy-Minh Le, *Le Quy Don Technical University, Hanoi, Vietnam.*

9:45 AM: **Register Grouping for Synthesis of Clock Gating Logic,** Inhak Han(1); Jonggyu Kim(2); Joonhwan Yi(2), Youngsoo Shin(1), *1: KAIST, Daejeon, Korea, 2: University of Kwangwoon, Seoul, Korea.*

9:55 AM: Coffee Break

# Session B – Reliability and Soft Error

## Tuesday, June 28th, 2016

## Session Chairs: Koji Eriguchi and Yuichiro Mitani

10:10 AM: *Invited* - **Layout Dependent BTI and HCI Degradation in Nano CMOS Technology: A New Time-Dependent LDE and Impacts on Circuit at End of Life**, Ru Huang; Pengpeng Ren; Runsheng Wang, Peking University, Beijing, China.

10:20 AM: **Accuracy of Quasi-Monte Carlo technique in Failure Probability Estimations**, Michail Noltsis(1); Dimitrios Rodopoulos(2); Pieter Weckx(2); Francky Catthoor(2); Dimitrios Soudris(1), *1: National Technical University of Athens, Greece; 2: imec, Belgium.*

10:30 AM: **An Area Compact Soft Error Resident Circuit for FPGA,** Motoki Amagasaki; Yuji Nakamura; Takuya Teraoka; Masahiro Iida; Toshinori Sueyoshi, *Kumamoto Univesity, Japan.*

10:40 AM: **Soft-Error Resilient Network-on-Chip for Safety-Critical Applications**, Khanh N. Dang; Yuichi Okuyama; Abderazek Ben Abdallah, *The University of Aizu, Japan.*

# Session C – I/O Circuits and ESD Protection

## Tuesday, June 28th, 2016

## Session Chairs: Lorenzo Cerati and Philippe Galy

10:50 AM: **A Method Of Leakage Reduction And Slew-Rate Adjustment in 2 x VDD output Buffer For 28 nm CMOS Technology And Above,** Tsung-Yi Tsai; Yan-You Chou; Chua-Chin Wang, *National Sun Yat-Sen University, Taiwan, Republic of China.*

11:00 AM: **Preliminary results on TFET - Gated diode in thin silicon film for IO design & ESD protection in 28nm UTBB FD-SOI CMOS technology**, Philippe Galy(1); Sotirios Athanasiou(2), *1: STmicroelectronics, France; 2: STmicroelectronics, IMEP, France.*

11:10 AM-12:01 PM: Workshop Sessions A, B & C

12:10 PM-1:05 PM: Lunch

1:05 PM *Keynote 2*- **Accelerating the Sensing World through Imaging Evolution**,
Yoshikazu Nitta, *Sony Semiconductor Solutions Corporation, Atsugi, Japan*

## Keynote 2:

Yoshikazu Nitta, Sony Corporation

Charge Coupled Device image sensors have made remarkable contributions to the performance and promotion of the camcorders and digital still cameras as key devices. CMOS Image sensors have provided high frame rate, low power consumption and high signal-to-noise ratio performance through the column-parallel analog-to-digital converters and back-illuminated technologies. With the introduction of these technologies, CMOS image sensors have widely used in not only mobile phones, but also surveillance cameras, industrial use and so on. As stacked CMOS image sensors continue to enhance functionalities, they can enlarge the value of image information in an image capturing field.

Evolution of CMOS imaging technologies, such as pursuing high sensitivity, high frame rate, and extending detectable wavelengths and depth resolution, will create attractive values in the present imaging world and the future sensing world.

# Session D: Advanced Transistors / Materials and High Power / High Voltage

## Tuesday, June 28th, 2016

## Session Chairs: Bich-Yen Nguyen and Wenke Weinreich

1:50 PM: *Invited* - **FDSOI Technology: Toward 0.3V CMOS Operation**, Olivier Webber, *STM, CEA-Leti, France.*

2:00 PM: **Extending HKMG scaling on CMOS with FDSOI: advantages and integration challenges**, Dina Triyoso(1); Rick Carter(1); Jon Kluth(1); Klaus Hempel(2); Michael Gribelyuk(1); Laegu Kang(1); Anil Kumar(1); Bob Mulfinger(1); Peter Javorka(2); Kasun Punchihewa(1); Amy Child(1); Tim McArdle(1); Judson Holt(1); Ryan Sporer(1); Sherry Straub(1); Paul Chen(1), *1: GLOBALFOUNDRIES USA; 2: GLOBALFOUNDRIES Germany.*

2:10 PM: **Characterization of High Pressure Hydrogen Annealing Effect on Polysilicon Channel Field Effect Transistors using Isothermal Deep Level Trap Spectroscopy**, Manh-Cuong Nguyen (1); An Hoang-Thuy Nguyen (1); Jae-Won Choi (1); Soo-Yeun Han (1); Jung-Yeon Kim(1); Rino Choi(1); Changhwan Choi(2), *1: Inha University, South Korea; 2: Hanyang University, South Korea.*

2:20 PM: *Invited* - **Beyond-Si materials and devices for more Moore and more than Moore applications–,** Nadine Collaert; A. Alian; H. Arimura; G. Boccardi; G. Eneman; J. Franco; Ts. Ivanov; D. Lin; J. Mitard; S. Ramesh; R. Rooyackers; M. Schaekers; A. Sibaya-Hernandez; S. Sioncke; Q. Smets; A. Vais; A. Vandooren; A. Veloso; A. Verhulst; D. Verreck; N. Waldron; A. Walke; L. Witters; H. Yu, X. Zhou; A. V.-Y. Thean, *IMEC, Belgium.*

2:30 PM: **Different Scalabilities of N- and P-Type Tunnel Field-Effect Transistors with Si/SiGe Heterojunctions**, Nguyen Dang Chien(1); Nguyen Thi Thu(2); Chun-Hsing Shih(3); Luu The Vinh(4), *1: Faculty of Physics, University of Dalat, Vietnam; 2: Department of Postgraduate Studies, University of Dalat, Vietnam; 3: National Chi Nan University, Taiwan, Republic of China; 4:Industrial University of Ho Chi Minh City, Vietnam.*

2:40 PM: **Organic Complementary Amplifier Circuits with Mixed Dielectrics for Large-area Active Collision Detection Sensors**, Toan Thanh Dao, *University of Transport and Communications, Vietnam.*

2:50 PM: **On-chip Accurate Primary-side Output Current Estimator for Flyback LED Driver Control**, Chua-Chin Wang; Zong-You Hou; Teng-Wei Huang, *National Sun Yat-Sen University, Taiwan, Republic of China.*

3:00 PM: Coffee Break

## Session E – RF&Analog Mixed Signal

### Tuesday, June 28th, 2016

### Session Chairs: Cuong Huynh and Dina Triyoso

3:15 PM *Invited* - **An Assessment On Low-Voltage Low-Power Integrated Single Transistor Active Inductor Design for RF Filter Applications,** Vincenzo Stornelli, *University of L'Aquila, Italy*

3:25 PM **A 4.2 mW 3.1 dBm IIP3 LNA in 0.13 µm CMOS for Wideband Communications,** Benqing Guo; Jun Chen; Haiyan Jin, *University of Electronic Science and Technology of China, People's Republic of China.*

3:35 PM **A 100-µW Wake-up Receiver for UHF Transceiver,** Phong Nguyen Thanh (1); Khanh Nguyen Tuan (2); Xuan Mai Dong (3),1,2: *Integrated Circuit Design Research and Education Center (ICDREC), Vietnam National University, Vietnam*; 3: *Ho Chi Minh City University of Technology (HCMUT), Vietnam National University, Vietnam.*

3:45 PM **A 65-nm CMOS High-Efficiency PWM/PFM Buck Converter with Bypass Mode for Transceiver Applications,** Duy Dang; Thang Tran Quoc; Kien Nguyen Van, *Integrated Circuit Design Research and Education Center (ICDREC), Vietnam.*

3:55 PM **A 200-mA CMOS Low-Dropout Regulator with High Current-Efficient and Transient-Response Improvement,** Nguyen Dinh Thuc, *Integrated Circuit Design Research and Education Center (ICDREC), Vietnam.*

4:05 PM **A 350uW 10-bit CMOS Cyclic D/A Converter with a Capacitor-Sharing Technique for Automatic Test Equipment,** Youngcheol Son; Jiwhan Oh; Yongjun Cho; Hyundong Kim; Minkyu Song, *Dongguk University, Seoul, Korea.*

4:15 PM – 5:15 PM: Workshop Sessions D & E

6:30 PM – 8:00 PM: Dinner Reception at Hotel Majestic Saigon

# Conference Program

## Wednesday, June 29th, 2016

8:00 AM Opening remarks (Yuichiro Mitani)

8:15 AM *Keynote3*- **Microprocessor: Past, Present, and Future**, Thang Tran, *Synopsys Inc., USA*

## Keynote3: Microprocessor: Past, Present, and Future

Thang Tran, Synopsys Inc.

Microprocessor is resilient with many lives. The first life is the high performance x86 microprocessor which is dominated by Intel and AMD. The second life is the low-power ARM microprocessor; ARM CortexA72 signified the end-of-life for ARM microprocessor. The next life is configurable microprocessor which is dominated by Synopsys and Cadence. ASIP is lurking in the future.

# Session F – SoC/MPSoC/SIP & CAD/DFX

## Wednesday, June 29th, 2016

## Session Chairs: Dac Pham, Juergen Pille, and Rouwaida Kanj

9:00 AM *Invited* - **Placement Optimization for MP-DSAL Compliant Layout,** Seongbo Shim (1, 2); Woohyun Chung (1); Youngsoo Shin (1); *1: Department of Electrical Engineering, KAIST, Daejeon 34101, Korea 2: Samsung Electronics, Hwasung 18448, Korea*

9:10 AM **A Digitally Controlled Oscillator Suitable for On-chip Integration in 65 nm CMOS,** Shanthi Sudalaiyandi; Gilles Mason; Mykhailo Zarudniev, *CEA LETI MINATEC, Grenoble, France.*

9:20 AM: **The Implementation of Homeplug AV system,** Ko-Chi Kuo, *National Sun Yat-sen University, Taiwan, Republic of China.*

9:30 AM: **Fast Design Exploration with Unified HW/SW co-verification Framework for High Throughput Wireless Communication System,** Nana Sutisna (1); Reina Hongyo (1); Leonardo Lanante Jr.(2); Yuhei Nagao(2); Masayuki Kurosaki(2); Hiroshi Ochi(2), *1: Graduate School of Computer Science and Electronics, Kyushu Institute of Technology, Japan; 2: Department of Computer Science and Electronics, Kyushu Institute of Technology, Japan.*

9:40 AM: **Routing-path Tracking and Updating Mechanism in Reconfigurable Network-on-Chips,** Thi-Thuy Nguyen; Thanh-Vu Le-Van; Xuan-Tu Tran; Hung K. Nguyen, *VNU University of Engineering and Technology (VNU-UET), Hanoi, Vietnam.*

9:50 AM: **The Design of a Phase Compensator for The CIC Decimation Filter,** Khanh Nguyen Quoc; Dong Bach Tuan; Toan Le Duc, *Integrated Circuit Design Research and Education Center (ICDREC), Vietnam.*

10:00 AM: **An All-in-One Debugger of 8-bit Microcontroller with High Transfer Speed,** Nguyen Hung Quan; Duong Hai Dang Linh; Trinh Viet Quang; Hoang Minh The Nghi; Nguyen Phu Quoc; Tran Kien Cuong; Hoang Xuan Hoa, *Integrated Circuit Design Research and Education Center (ICDREC), Vietnam.*

10:10 AM: Coffee Break

## Session G - Advanced Memory Devices

### Wednesday, June 29th, 2016

### Session Chair: Hideto Hidaka

10:30 AM *Invited* - **Highly Reliable Anti-Fuse Technology in sub-16nm Technologies for Security Applications,** Rick Shen; Hsin-Ming Chen; Meng-Yi Wu, *eMemory Technology Inc., Taiwan, Republic of China.*

10:40 AM *Invited* - **Scaling of Split-Gate Flash Memory and its Adoption in Modern Embedded Non-Volatile Applications,** Nhan Do, *Microchip Technology Inc., USA.*

10:50 AM **An Ultra-Low Power Operated Logic NVM for Passive UHF RFID Tag Applications**, Wu-Chang Chang; Po-Ching Wu; Cheng-Hao Po; Chun-Fu Lin; Ching-Yuan Lin; Chih-Hsin Chen, *eMemory Technology Inc.Taiwan, Republic of China.*

11:00AM **Dynamic CMOS-Rectifying memristor multiplier architecture for power reduction,** Huan Minh Vo, *Ho Chi Minh city University of Technology and Education, Vietnam.*

11:10 AM **71% lossless compression of memory bandwidth for a multi-standard video codec by combination of 2D-DPCM and Variable Length Coding**, Chi Lan Phuong Nguyen81); My Phi Ngoc Nguyen (1); Hung Van Cao (1); Katsushige Matsubara (2); Keisuke Matsumoto (2); Seiji Mochizuki (2); Kenichi Iwata (2), *1: Renesas Design Vietnam Co., Ltd., Ho Chi Minh City, Vietnam, 2: Renesas System Design Co., Ltd., Tokyo, Japan.*

11:20 PM – 12:20 PM: Workshop Sessions F & G

12:20 PM - 1:20 PM: Lunch

1:20 PM *Keynote4*-**Minimal Fab: a small semiconductor factory free from huge investment**, Sommawan Khumpuang, *AIST,Japan*

## Keynote4:

Sommawan Khumpuang, National Institute of Advanced Industrial Science and Technology (AIST)

The minimal fab concept was designed in order to achieve brand-new semiconductor fab whose investment cost is 1/1,000 of a conventional mega fab. The targets of minimal fab are device markets with high-variation and low-volume. The minimal fab has three important features. (1) The wafer diameter is a half inch. (2) Each process tool size is 294 mm wide × 450 mm deep × 1440 mm high. (3) No clean room is needed due to the use of local clean technology. This paper describes the concept, development of minimal equipment, and the fabrication of devices using the equipment.

# Session H - Minimal Fab Application

**Wednesday, June 29th, 2016**

**Session Chairs: Dang Luong Mo and Sommawan Khumpuang**

2:05 PM *Invited* - **Development of Fundamental Manufacturing Processes for Minimal Fab.**, Sommawan Khumpuang; Shiro Hara, *National Institute of Advance Industrial Science and Technology (AIST).*

2:15PM: **Blue GaN based LED Fabrication using Hybrid Process of the Minimal Photolithography System and MOCVD,** Masanori Iwata; Kenji Miyake; Nobuyoshi Yamauchi; Junko Kazusa, *PMT Corporation, Fukuoka, Japan.*

2:25 PM: *Invited* - **Packaging in Minimal Fab**, Michihiro Inoue; Fumito Imura; Arami Saruwatri; Shiro Hara, *National Institute of Advance Industrial Science and Technology (AIST).*

2:35 AM: Coffee Break

# Session I – 3D Integration & Emerging Technologies

**Wednesday, June 29th, 2016**

**Session Chairs: Thomas Ernst and Thuy Dao**

2:55 PM *Invited* - **Monolithic 3D Integration,** Claire Fenouillet-Beranger; Maud Vinet, *CEA-Leti, France.*

3:05 PM **La-doped ZrO2 based BEoL decoupling capacitors**, W. Weinreich (1); K. Seidel (1); P. Polakowski (1); M. Drescher (1), A. Gummenscheimer (2); M.G. Nolan (2); L. Cheng (3); D.H. Triyoso (3), *1: Fraunhofer IPMS-CNT, Dresden, Germany, 2: GLOBALFOUNDRIES, Dresden, Germany, 3: GLOBALFOUNDRIES, Malta, USA.*

3:15 PM *Invited* - **2.5D Interposer implementation**, Kar Yee Tang, *eSilicon, USA.*

3:25 PM *Invited* - **Improved electrical and thermal performances in nanostructured GaN devices**, Jun Ma, *École polytechnique fédérale de Lausanne (EPFL), Switzerland.*

3:35 PM **Exploration and Evaluation of Hybrid TFET-MOSFET Monolithic 3D SRAMs Considering Interlayer Coupling**, Jian-Hao Wang; Yin-Nien Chen; Pin Su; Ching-Te Chuang, *National Chiao Tung University, Taiwan, Republic of China.*

3:45 PM **Conductive Polymer/Metal Composite for Flexible Interconnect**, Jin Kawakita; Toyohiro Chikyow, *National Institute for Materials Science, Japan.*

3:55 PM – 4:55 PM: Workshop Sessions H & I

4:55 PM: Best student paper award

5:10 PM – 5.25 PM: Closing Remarks & Presentations of ICICDT 2017

6:00 PM – 8:00 PM: Post-conference Meeting for TPC